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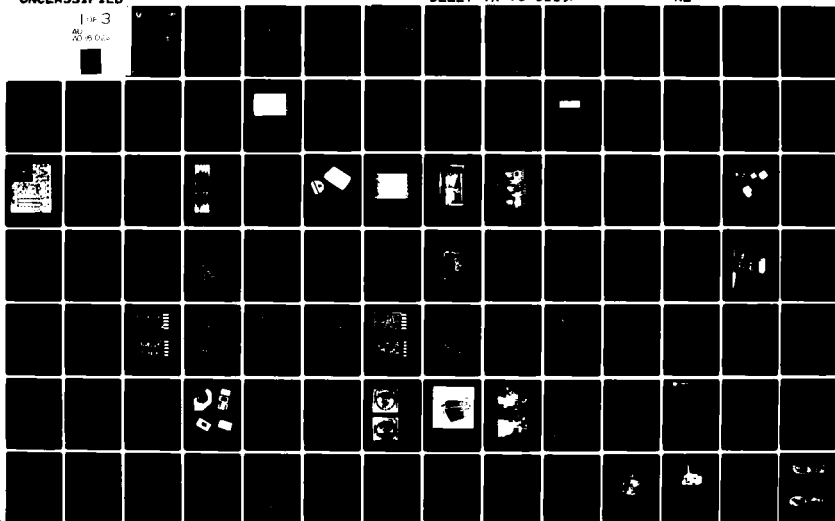
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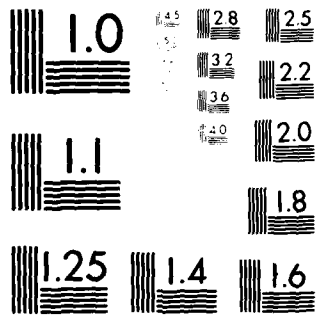
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# Research and Development Technical Report

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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING  
(MM & TE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION  
TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS  
USED IN CRYSTAL OSCILLATORS

VOLUME I

R. Michel Zilberstein

RAYTHEON COMPANY  
Industrial Components Operation  
Quincy, MA 02169

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JUN 27 1980

April 1980

Final Report for Period August 1976 - August 1979

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⑥ **MANUFACTURING METHODS AND TECHNOLOGY  
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ESTABLISHMENT OF PRODUCTION TECHNIQUES  
FOR HIGH DENSITY THICK FILM CIRCUITS USED  
IN CRYSTAL OSCILLATORS.**

Volume I.

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⑪ **APR 1980**

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⑨ Final rept. 6 Aug 76 - Aug 79

**Prepared by**

⑩ **R. MICHEL/ZILBERSTEIN**

⑮ DAAB07-76-C-2117

**ACKNOWLEDGEMENT STATEMENT**

This project has been accomplished as part of the U S Army Manufacturing and Technology Program which has as its objective the timely establishment of manufacturing processes, techniques, or equipment to ensure the efficient production of current or future defense programs.

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detailed layout design of the hybrid microcircuitry used in the TCVCX0 module; the detailed design of piece parts to be used to seal the hybrid microcircuits and to encapsulate the modules; the establishment of process flow plans to produce the modules; and the selection, characterization, and procurement of component parts and materials required for the production of the TCVCX0 modules. The Production phase involved the development of tooling and manufacturing techniques needed to achieve the program requirements; and the delivery of completed modules in accordance with the program schedule.

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## **1.0 INTRODUCTION**

This final report covers the work conducted by Raytheon Company, Industrial Components Operation, in the course of a three-year Manufacturing Methods and Technology Engineering Program carried out under the terms of Contract No. DAAB-76-C-8119. The objectives of the program were:

- a. To establish production techniques for high-density, thick-film, hybrid microcircuits to be used in crystal oscillators, and
- b. To produce specified quantities of a 20 MHz, temperature-compensated, voltage-controlled, quartz crystal oscillator (TCVCXO) utilizing the techniques developed in a.

This report defines the program requirements and details Raytheon's program plan to meet those requirements. The technical approach and its implementation, as well as recommendations for future development, are discussed in detail.

The Engineering Phase of this Manufacturing Methods and Technology Engineering program consisted on the following tasks:

1. Electrical breadboard construction
2. Breadboard evaluation
3. Module configuration design
4. Process flow plan generation
5. Hybrid microcircuit parts selection
6. Hybrid microcircuit parts and bonding tools procurement
7. Thick-film processing materials procurement
8. Potting shells and encapsulant materials procurement
9. Hybrid microcircuit layout design
10. Layout artwork generation
11. Thick-film printing screen procurement

12. Assembly drawing generation
13. Assembly materials procurement
14. Assembly process development
15. Encapsulation process development
16. Hermetic sealing process development
17. Hermetic sealing parts and materials procurement
18. Test flow plan generation
19. Test procedure generation
20. Test fixture design and fabrication
21. Thick-film substrate fabrication
22. Passive and active laser trimming procedure development
23. Substrate assembly (10-lot)
24. Electrical testing of substrate assemblies (preseal tests) (10-lot)
25. Hermetic sealing of substrate assemblies (10-lot)
26. Leak testing of hermetically sealed substrate assemblies (10-lot)
27. Module assembly (10-lot)
28. Electrical testing of assembled module (pre-aging) (10-lot)
29. Module aging (10-lot)
30. Electrical testing of modules (final tests) (10-lot)
31. Substrate assembly (15-lot)
32. Electrical testing of substrate assemblies (preseal tests) (15-lot)
33. Hermetic sealing of substrate assemblies (15-lot)
34. Leak testing of sealed substrate assemblies (15-lot)
35. Module assembly (15-lot)
36. Electrical testing of assembled modules (prepot tests) (15-lot)
37. Module encapsulation (15-lot, as required)
38. Electrical testing of encapsulated modules (post-pot tests) (15-lot, as required)
39. Module aging (15-lot)
40. Electrical testing of modules (final tests) (15-lot).

## 1.1 Basic Theory of Operation

The need for portable, battery-operated, remote battlefield sensing devices and similar military hardware has mandated the development of lightweight, low-power, high-stability, highly shock and vibration-resistant crystal oscillators. The purpose of this project was to develop such components by combining the proven stability under shock and vibration of ERADCOM-developed ceramic-packaged quartz crystal resonators<sup>1,2</sup> with the reliability and high-production capability of thick-film hybrid technology. Frequency, established by a quartz crystal, is in the 17 to 22 MHz range; output wave-shape is quasi-sinusoidal. The unit has the capability for frequency-shift keying (FSK) and analog modulation; deviation sensitivity is nominally 500 Hz per volt, and linearity is better than 5%. The device is energized by a single, 12-volt (nominal) power supply, and dissipates a maximum power of 50 milliwatts. Physically, the diallyl phthalate-cased TCVCXO assumes the geometry of a truncated cylinder and is designed to be inserted directly into a printed-circuit-board-type strip connector (Figure 1.1). The operating temperature range is  $-40^{\circ}$  to  $+75^{\circ}\text{C}$ . An externally adjustable frequency trimmer potentiometer is accessible through a recessed opening. Detailed specifications for the unit appear in ERADCOM document SCS-483 (Appendix A of this report) and in Amendments thereto.

The functional block diagram of the TCVCXO is shown in Figure 1.2 and a final schematic in Figure 1.3. The oscillator stage consists of a modified antiresonant Pierce crystal oscillator (Figure 1.4) which contains a voltage-dependent capacitor (varactor, VVC Diode) in series with the crystal. The output frequency is dependent upon the voltage impressed across the varactor; hence temperature-induced frequency variations can be compensated for by applying the appropriate correction voltage across the varactor. Likewise, modulation of the oscillator frequency is achieved by applying the modulation voltage (appropriately transformed, as required) to the varactor. The

1. Ceramic Flat Pack Enclosures for Precision Quartz Crystal Units, by R. Donald Peters, Proc. 30th Annual Symposium on Frequency Control, pp. 224-231 (1976).
2. Polyimide Bonded Resonators, by R.L. Filler, J.M. Frank, R.D. Peters, and J.R. Vic, Proc. 32nd Annual Symposium on Frequency Control, pp. 290-298 (1978).

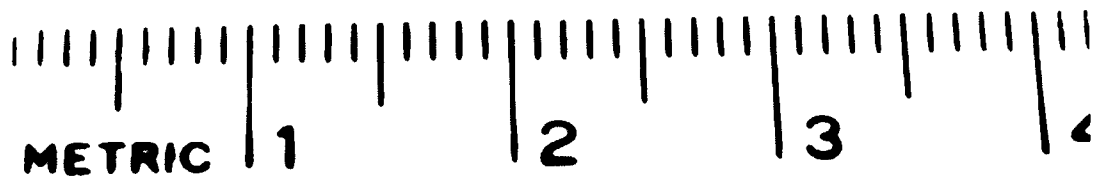
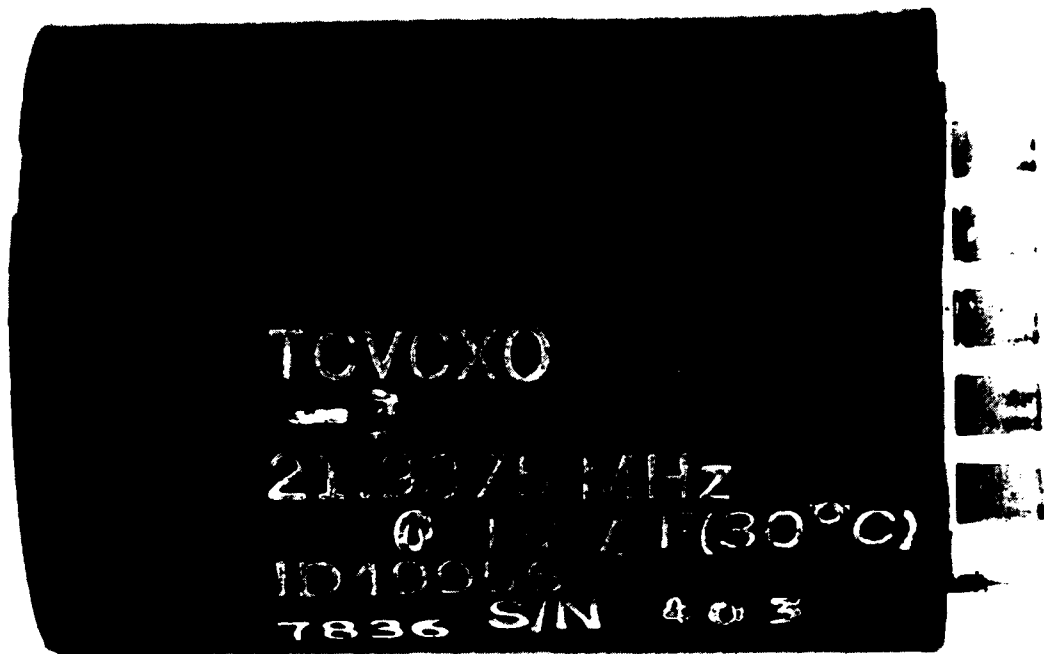


Figure 1.1 TCVCXO Final Configuration

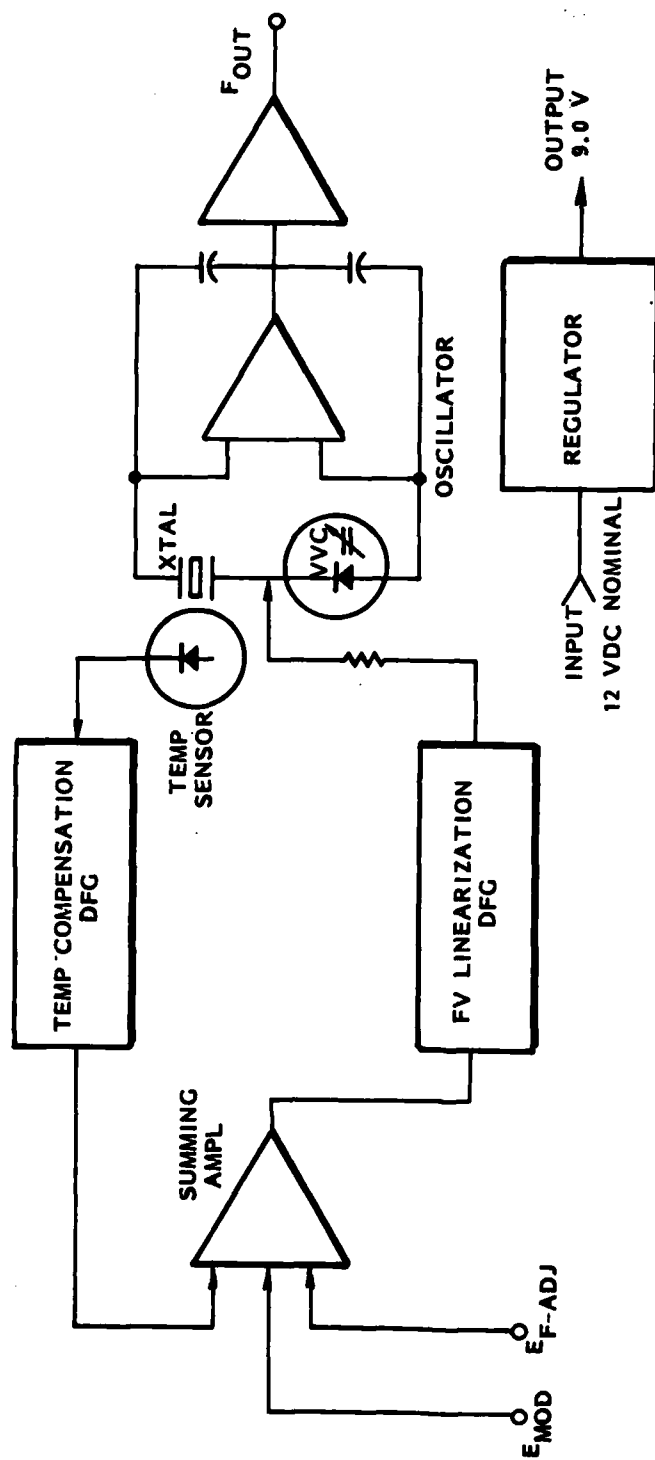


Figure 1.2 TCVCXO Functional Block Diagram



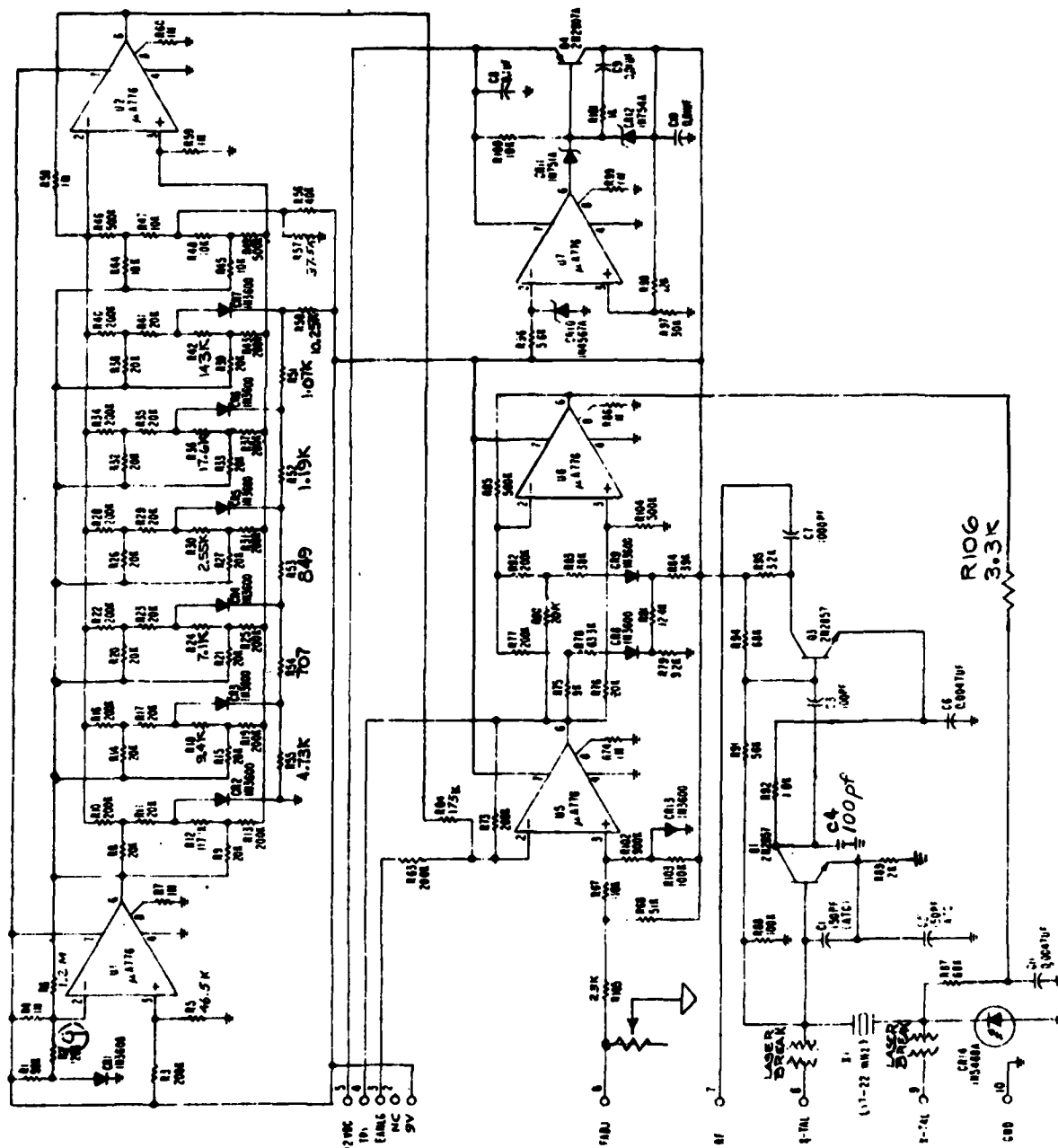


Figure 1.3 TCVCXO Final Schematic

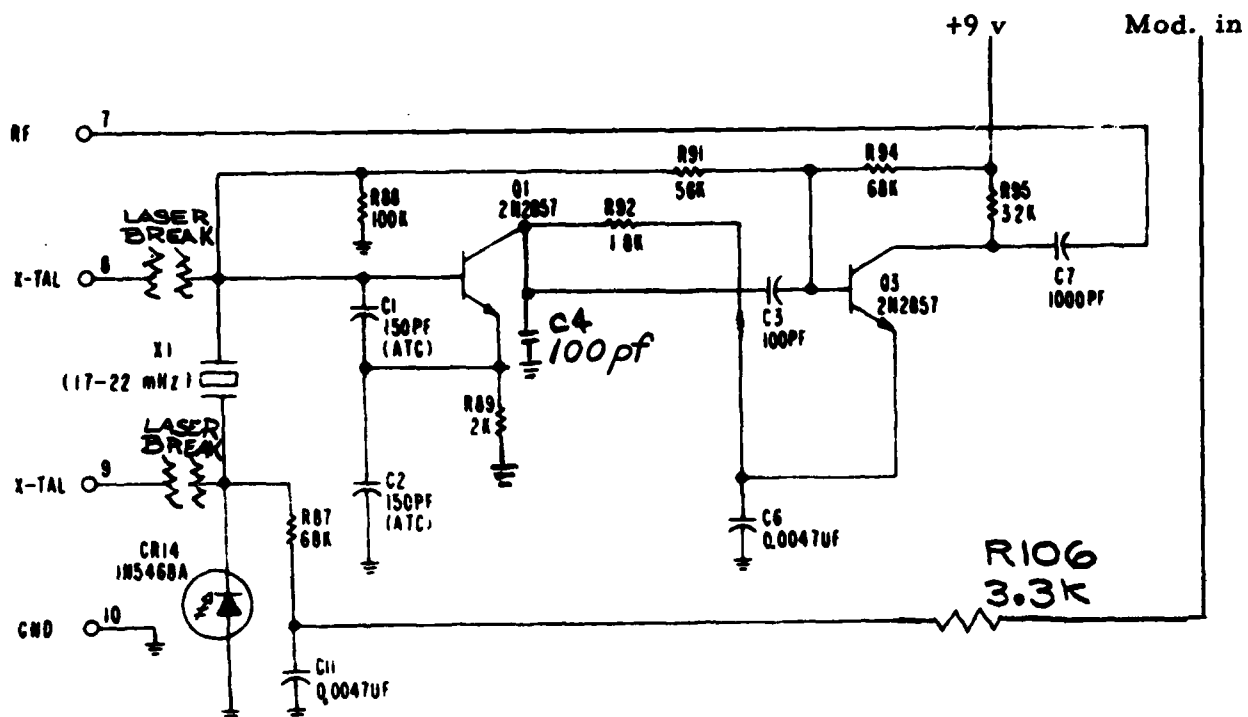


Figure 1.4 TCVCXO Schematic, Oscillator Section

inherent stability of the design has been ensured by the elimination of inductors from the circuit. A single-stage buffer (Q3) isolates the oscillator from the load and provides additional gain. Power consumption is minimized through the use of a stacked design.

The crystal resonator originally intended for this application is specified in ERADCOM Technical document SCS-512 (See Appendix B). It is a high shock and vibration-resistant unit vacuum-sealed in a ceramic package. Rigorous process control and material selection guarantee a very low aging rate. The resonator blank is a deep-etched, gold-electroded, fundamental mode AT-cut quartz crystal designed to function in the parallel mode with a load capacity of 20 pF. The temperature versus frequency characteristic of the crystal determines that of the oscillator; for typical AT-cut crystals, it approximates a cubic function, with turnover temperatures and frequency deviations determined by the angle of cut of the quartz blank with respect to the axes of the mother crystal (Figure 1.5).

Delivery problems with the ceramic-cased crystals dictated the use of other configurations during the performance of this contract; while mechanical characteristics differed somewhat, electrical parameters were essentially the same.

Linearization of the varactor voltage vs. oscillator frequency relationship is effected by means of a diode function generator (DFG) which produces a two-segment voltage transfer function approximating the inverse of the oscillator's frequency-versus-voltage characteristic. Using the DFG to process the modulation signals applied to the unit permits the attainment of better than 5% linearity over a deviation range of 100 ppm. Similarly, the temperature correction and frequency trim voltages derived respectively from the TCFG circuit and a voltage divider incorporating an externally adjustable potentiometer are applied to the tuning varactor after processing by the DFG linearizing circuit.

Frequency-temperature compensation is obtained with a 6-segment DFG which generates a cubic transfer function approximating the reverse of an AT-cut crystal frequency-versus-temperature characteristic. The circuit incorporates a capability

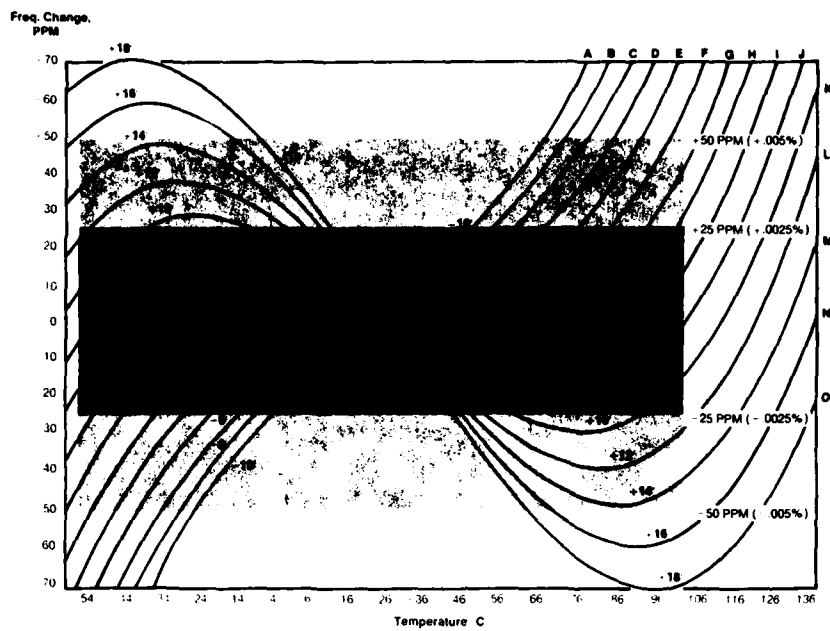


Figure 1.5 AT-Cut Quartz Crystal Frequency vs Temperature Characteristics

for rotating the slope of the linear region, thus making possible the correction of any crystal deviation from the ideal F/T curve. A silicon diode is used as the temperature sensor. This portion of the circuit is designated as the Temperature Compensation Function Generator (TCFG).

Regulated power (essential for oscillator stability) is obtained through the use of a voltage regulator consisting of a low-power operational amplifier and a 0.5 mA temperature-compensated reference diode. Load regulation problems arising from output current limitations in the operational amplifier are avoided through the use of an external pass transistor. Control of the AC gain of the transistor stage through the use of RC networks suppresses potential oscillations and guarantees stability. The regulator provides an output voltage of 9.00 V with an input voltage range of 10 to 15 volts over the full operating temperature range.

Laser trimming of resistors is prescribed to attain the component tolerances dictated by the specification. Initially, the 105 fixed resistors in the design are passively trimmed to a 5% tolerance. Subsequently, 12 resistors are actively laser-trimmed while the functions which they control are monitored. An Operational Laser Trimming program was supplied by ERADCOM and served as a basis for the final trimming procedure adopted by Raytheon.

## 2.0 PROGRAM OBJECTIVES

Raytheon has implemented this manufacturing methods and technology engineering program in accordance with Electronics Command Industrial Preparedness procurement requirements for Technical Requirement SCS-483 (Appendix A), which specifies a hermetically-sealed 17 MHz to 22 MHz temperature-compensated, voltage-controlled crystal oscillator (TCVCXO). The objective of the Industrial Preparedness program is to establish a production capability to meet estimated military needs for a period of two years after completion of the MM&TE program, and to establish a base and plans which may be used to meet expanded production requirements. The objectives of the subject MM&TE program were: to establish the producibility of the TCVCXO module by mass production techniques and with mass production facilities; to establish a quality control system for production; to develop procedures to reduce the time required for delivery of modules in large quantity; and to demonstrate a production rate of 125 units per week.

During the performance of this MM&TE contract, a production contract (DAAB07-78CA116) was awarded by ERADCOM for the delivery of 500 TCVCXO modules.

Because of the contract overlap, engineering and manufacturing developments, while kept separate for accounting purposes, were freely interchanged between the two contracts. Accordingly, final conclusions, process descriptions, test procedures, and tooling designs are based not only on work performed specifically on the MM&TE contract, but also on the results of the experience acquired on the production contract.

The combined MM&TE and production programs encompassed the following tasks:

- a. Performance of the necessary design and development engineering, tool design, test facilities construction, and production equipment selection, as required, to obtain confirmatory sample approval, establish a pilot line and make a pilot run for proving out a manufacturing process using production methods and techniques.

- b. Completion of all production planning needed for compliance, initially, with the schedule for MM&TE module delivery requirements; and, finally, with the production contract requirements.

TCVCXO modules were to be fabricated and delivered on the MM&TE program in four lots as follows:

Engineering Samples

First Submission	10 Each
Second Submission	15 Each
Confirmatory Samples	50 Each
Pilot Run Units	100 Each

The primary technical objective was the development of thick-film approaches to TCVCXO construction to yield a device capable of meeting the physical, mechanical, and electrical requirements of document SCS-483, within the cost guidelines imposed by ERADCOM. Design and construction were to conform to MIL-M-38510. The unit was to incorporate the high reliability ceramic-packaged quartz crystal resonator developed at ERADCOM, and utilize beam-leaded devices wherever possible. Passive and active resistor trimming were to be accomplished using a programmable laser trim system.

Throughout the course of the program, changes in scope and in both mechanical and electrical specifications were prescribed, some at ERADCOM's initiative, others upon Raytheon's request. The impact of these changes will be presented in detail in this report.

### 3.0 ELECTRICAL DESIGN ANALYSIS

The electrical design of the TCVCXO, as originally defined in ERADCOM's technical requirement SCS-483, and subsequently modified by ERADCOM through several amendments, was breadboarded at Raytheon at the start of the Engineering Phase. The objectives in so doing were:

- a. to obtain a working familiarity with the electrical design and performance before proceeding to microcircuit design, fabrication, and testing;
- b. to acquire a vehicle to develop test procedures and set-ups for use in subsequent module testing;
- c. to evaluate component performance in the final circuit; and,
- d. to obtain a means to diagnose electrical faults in defective modules by recreating failure symptoms in the breadboard.

The breadboard was built using standard discrete components, with the exception of the two capacitors C1 and C2 in the oscillator stage.

To achieve best possible correlation between breadboard performance and final circuit behavior, the actual porcelain capacitors intended for use in the hybrid were used on the breadboard (Figure 3.1).

The basic approach pursued in testing the breadboard was, first, to obtain an operating circuit; to implement the resistor functional trim procedure; and then to check the performance of the breadboard against the specifications in SCS-483.

Progress was impeded in the beginning by a problem encountered with spurious oscillations in the breadboard and then with a distorted rf output voltage waveform.



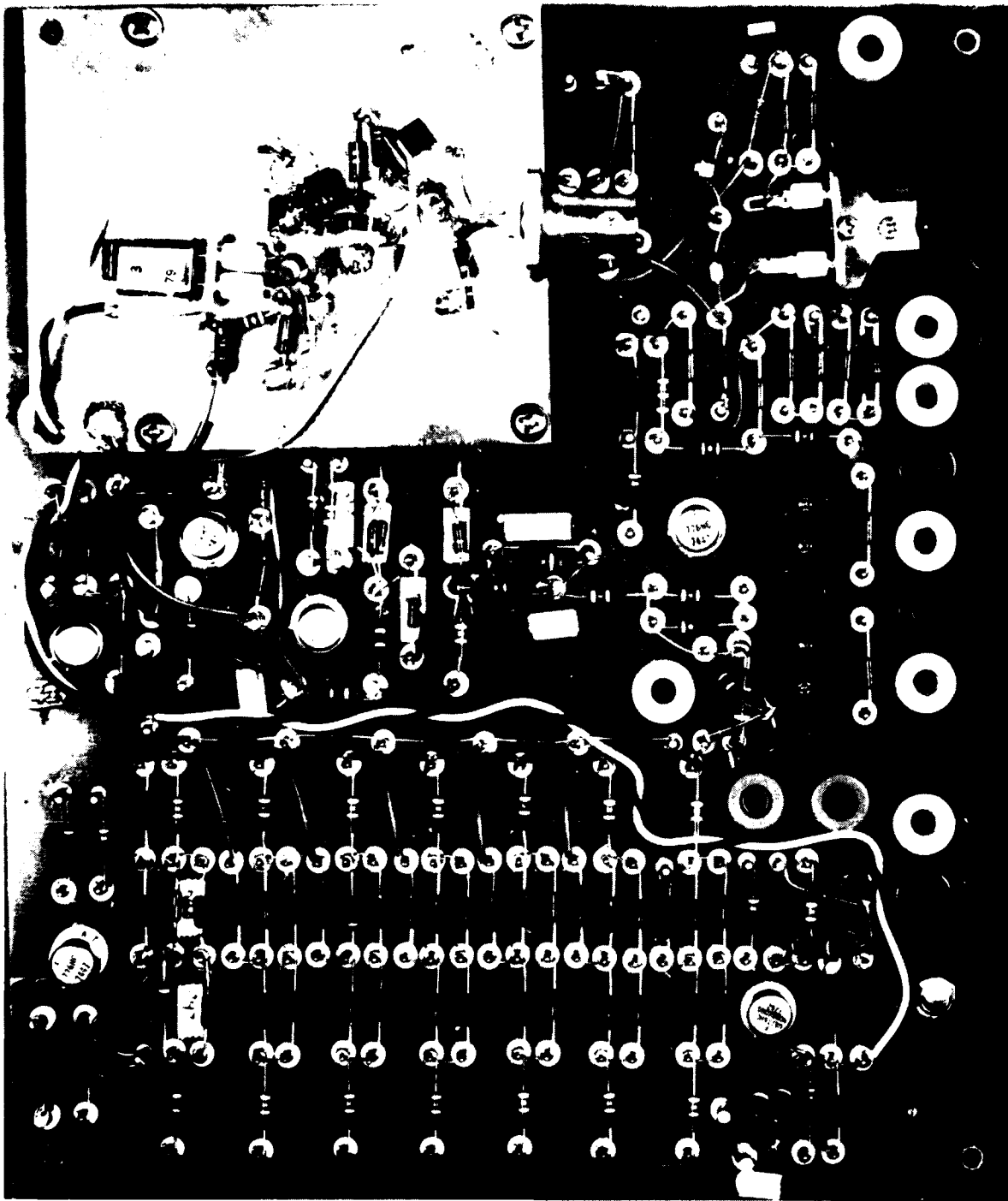


Figure 3.1 TCVCXO Breadboard

The spurious oscillation problem was eventually solved by a slight change in breadboard layout and by grounding the transistor cases in the oscillator stage. The distorted output turned out to be characteristic of the electrical design, and hence solvable only by a change in design. This was not attempted since development of the electrical design was outside of the scope of this program.

Another significant problem encountered early in breadboard testing was a limited modulation capability. As the oscillator stage was laid out, stray capacitances tended to swamp out the effect of the variable capacitance diode CR14 and therefore limited the shift in frequency achievable by modulation. A layout revision solved the problem.

Inherent limitations in the breadboard layout prevented complete performance testing of the circuit to the specifications, particularly with respect to temperature stability. However, the resistor functional trimming procedure was evaluated fully, and the results were used in the final layout design.

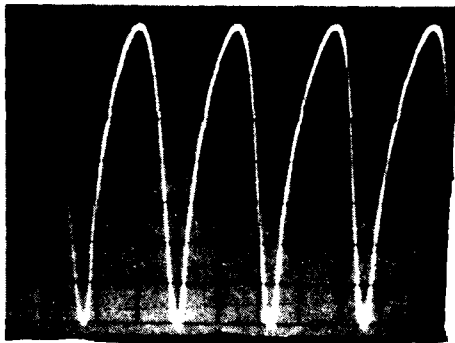
A summary of the accumulated observations on the breadboard layout leads to the following conclusions:

- a. The oscillator stage layout must be very tight in order to reduce stray impedances;
- b. The temperature-sensing diode, CR1, must be located physically in close proximity to the crystal in order to achieve proper temperature compensation;
- c. The VCXO deviation linearity appears marginal. Apparently the one break-point in the linearization network is not sufficiently effective. A redesigned network with two or more break-points would seem to be required in future designs.

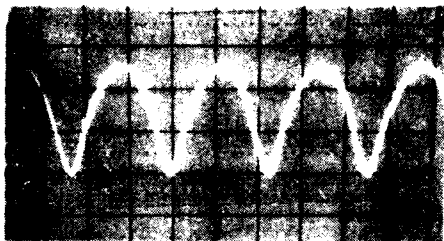
- d. The frequency adjustment range appears to be excessive with the crystals provided for the test, resulting in rather high adjustment sensitivity. This limitation could be remedied by circuit redesign, crystal redesign, or both;
- e. The rf voltage waveform is not sinusoidal;
- f. Oscillator transient frequency stability is within 2 Hz from 5 ms to 100 ms after initial turn-on;
- g. The 9-volt regulator output varies  $-0.003\%$  C. A 40 mV change in the 9-volt supply causes a  $-0.5$  ppm frequency shift.
- h. It is necessary to follow precisely the ERADCOM 12-step functional trim procedure for resistors in order to achieve adequate temperature compensation.

These conclusions were confirmed, in general, by the performance of completed modules. Additionally, the temperature performance of the hybrid components, as anticipated, was better than that of the breadboard.

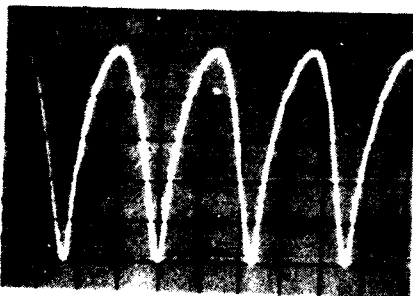
Some of the difficulties encountered with hybrid modules in the course of production were analyzed with the aid of the breadboard. Specifically, low output amplitude characteristics were correctly ascribed to low  $h_{fe}$  transistors in the oscillator and buffer stages of the TCVCXO (Figure 3.2). These tests aided in the formulation of acceptance standards for these components. The breadboard was also used in later stages of production to determine the effects of crystal characteristics on oscillator performance, and to attempt to establish relationships between heretofore unavailable crystal test parameters and various TCVCXO failures. Causes of transient frequency stability failures remain elusive, despite attempts to simulate the problem on the breadboard. It must be remembered that this method of fault analysis suffers from the fact that while all discrete components used in the breadboard can be characterized in full prior to assembly, chip components used in the final hybrid circuit package cannot be so tested.



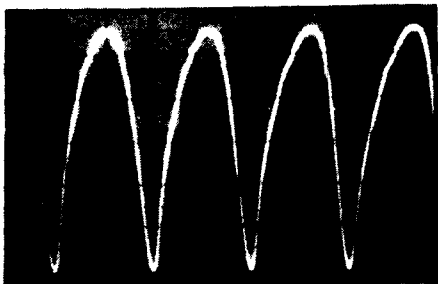
Osc. Transistor Beta : 100  
Buffer Transistor Beta : 90



Osc. Transistor Beta : 25  
Buffer Transistor Beta : 25



Osc. Transistor Beta : 90  
Buffer Transistor Beta : 25



Osc. Transistor Beta : 50  
Buffer Transistor Beta : 50

Figure 3.2 Transistor  $H_{fe}$  Effect on Output Amplitude

## 4.0 TECHNICAL APPROACH

### 4.1 Module Configuration and Construction

From the inception of the project, the TCVCXO was conceived as consisting of two hermetically sealed hybrid microcircuit substrate assemblies mounted back-to-back, electrically mated via interconnecting straps, and encapsulated in the form of a truncated cylinder. The rather complex module outline is best accomplished through the use of a precast potting shell filled with a low-density epoxy resin. The use of a cover over the plug-in end eliminates the need for any finishing operation after potting (Figure 4.1).

To guarantee parts commonality and to minimize duplication in process tools and fixtures, a common substrate size was chosen for both submodules. Hermetic sealing of the two substrates is accomplished through the use of alumina corrals and flat metal covers. Again, to reduce tooling and manufacturing costs, the corral cross-sectional dimensions are identical (but the heights are different) and the metal covers are interchangeable (with exceptions to be noted later). The alumina corrals are sealed to the processed thick-film alumina substrate with a conventional solder glass. The upper surface of the corral is metallized and has a Kovar frame brazed to it. The flat Kovar cover is then sealed to the frame by parallel-seam welding (Figure 4.2).

The two hybrid microcircuits are mated by bonding with an epoxy preform (Ablefilm 550 Epoxy Film Adhesive). The potentiometer assembly is epoxied to the metal cover of the VCXO submodule (Figure 4.3). While the original concept called for a ceramic-packaged crystal to be mounted within the sealed corral, procurement problems resulted in the utilization of three different crystal types (Figure 4.4) which were also epoxied to the metal cover of the VCXO module. Space constraints forced some cover modifications for certain types of metal crystal packages.

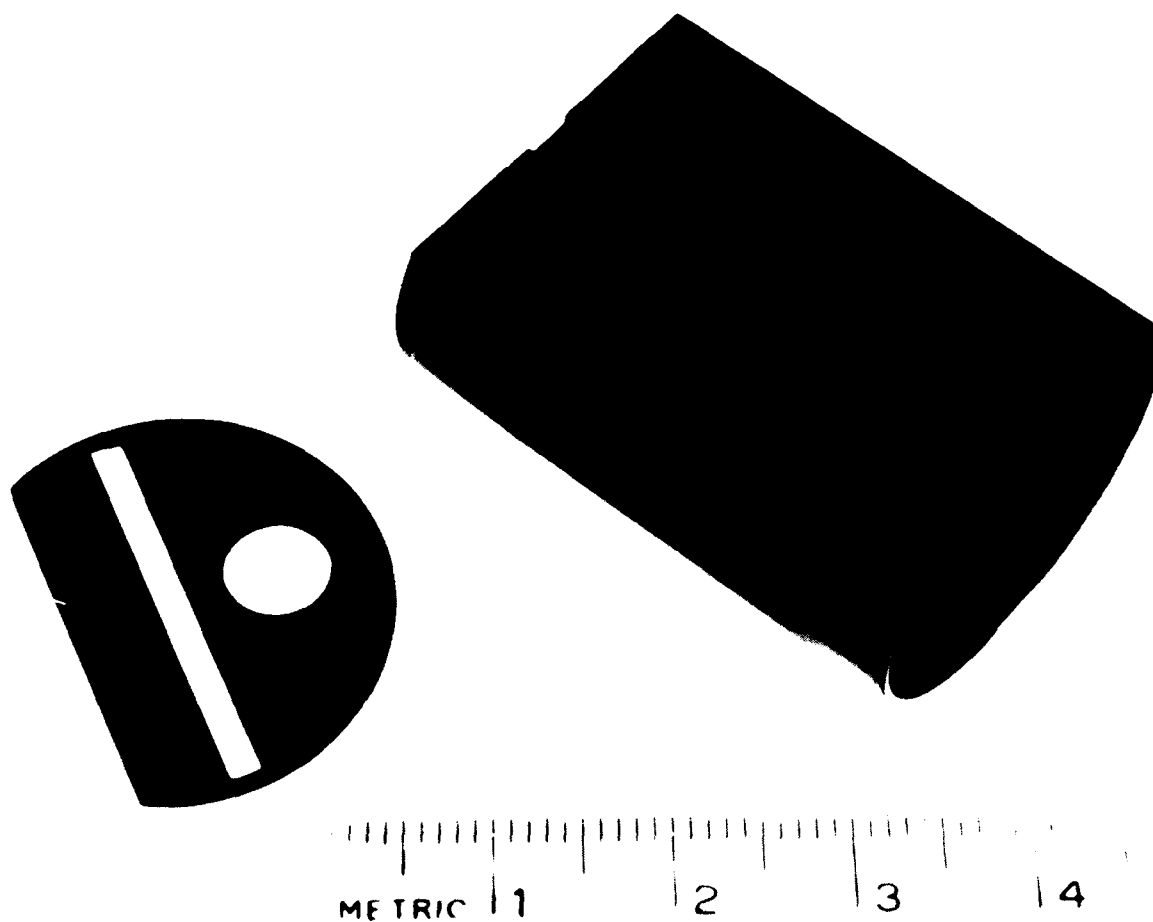


Figure 4.1 TCVCXO Potting Shell and Cover

# Sealing

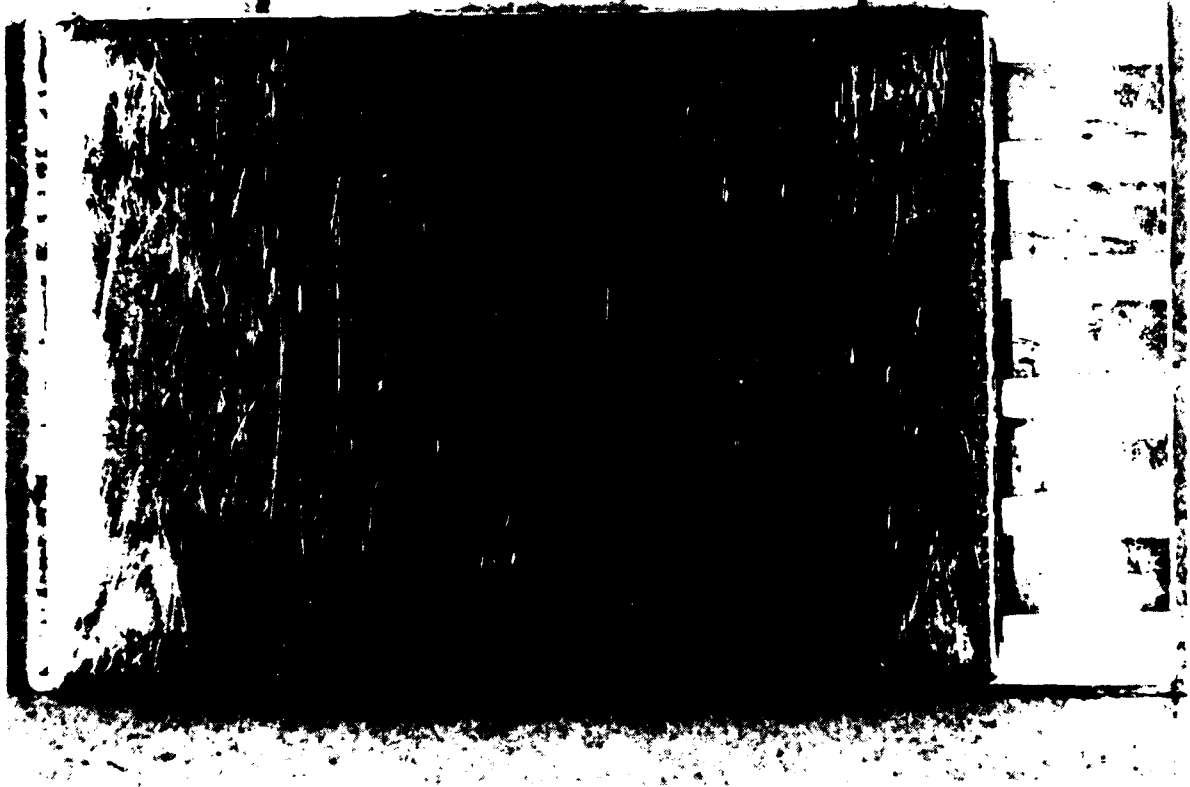


Figure 4.2 TCVCXO Sealed Corral



Figure 4.3 TCVCXO Potentiometer Assembly in Place





Figure 4.4 TCVCXO Three Alternate Crystal Configurations

Two major mechanical modifications were required by ERADCOM after the contract award:

- a. A provision for extracting the module from its socket where essentially only the end of the module opposite the socket is accessible, and;
- b. Protection of the frequency-adjust potentiometer adjustment screw from moisture.

The requirement for a means of extraction stems from the fact that the cylindrically shaped module, in its system application, seats snugly in a hole, with the socket located at the bottom of the hole. The sides of the module are not accessible for hand removal; consequently, a provision for module extraction was developed involving the combined use of T-shaped slots in the potting shell exterior surface (Figure 4.5) and a special extraction tool (Figure 4.6). One of the slots is so designed that, in an emergency, the module is extractable with the aid of a simple bent wire hook.

To meet the moisture protection requirement, a bushing was designed to encircle the potentiometer adjust screw, enclosing it in the region between the potentiometer body and the potting shell wall. The bushing is internally threaded to accept a nylon set-screw which provides the moisture seal. Removal of the set-screw exposes the potentiometer adjustment screw (Figure 4.7).

#### 4.2 Hybrid Microcircuit Partitioning

The electrical circuit for the TCVCXO was partitioned into two major functional parts, designated as the linearized voltage-controlled crystal oscillator (VCXO) section, and the temperature-compensated diode function generator (TCFG) section; the VCXO submodule also contains the voltage regulator. Partitioning was based on circuit interrelationships and the need to minimize the number of interconnections between the two substrates. The partitioning scheme, as it relates to the final version of the TCVCXO module, is shown in Figure 4.8.

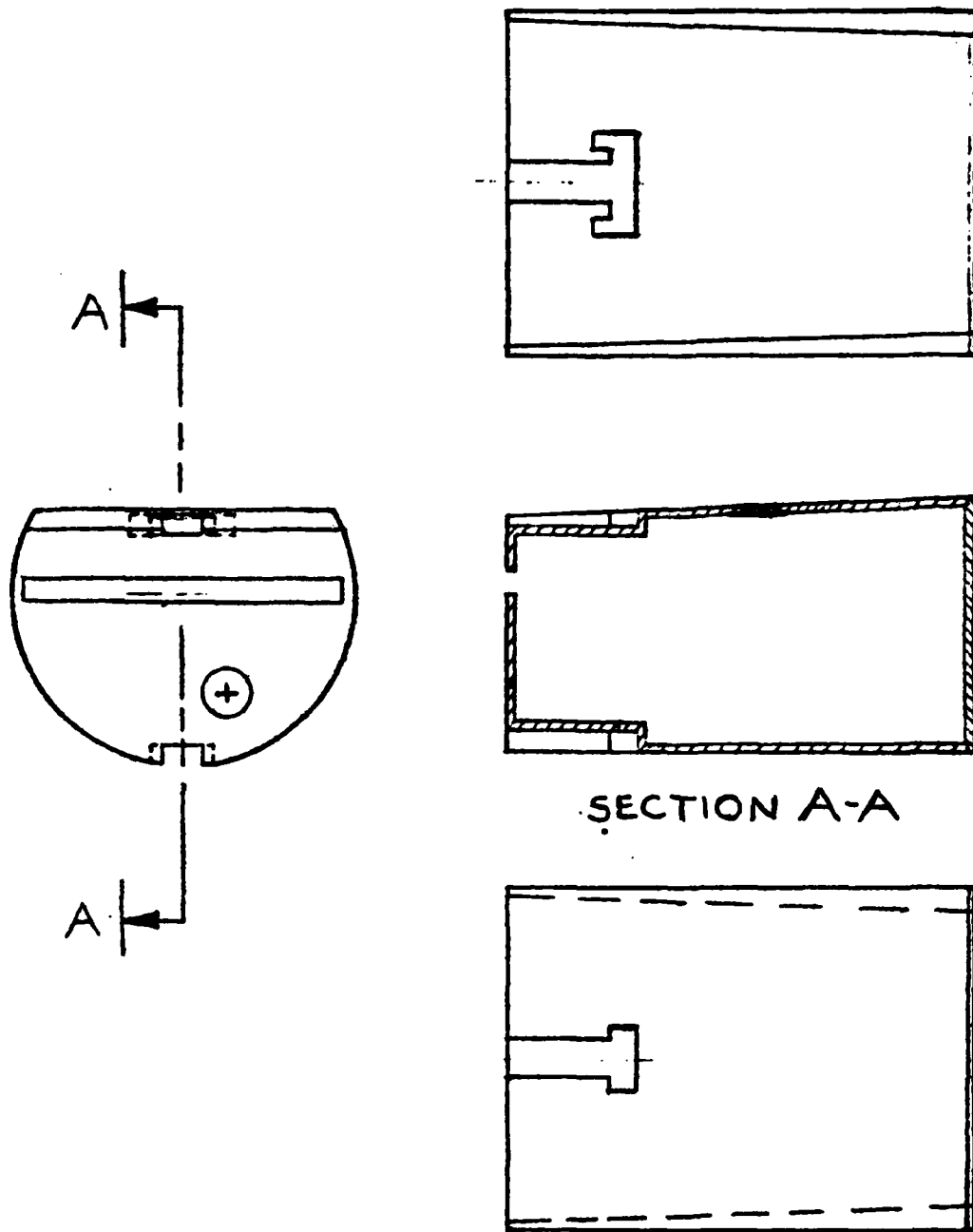


Figure 4.5 TCVCXO Diallyl Phthalate Case, with Extraction Slots

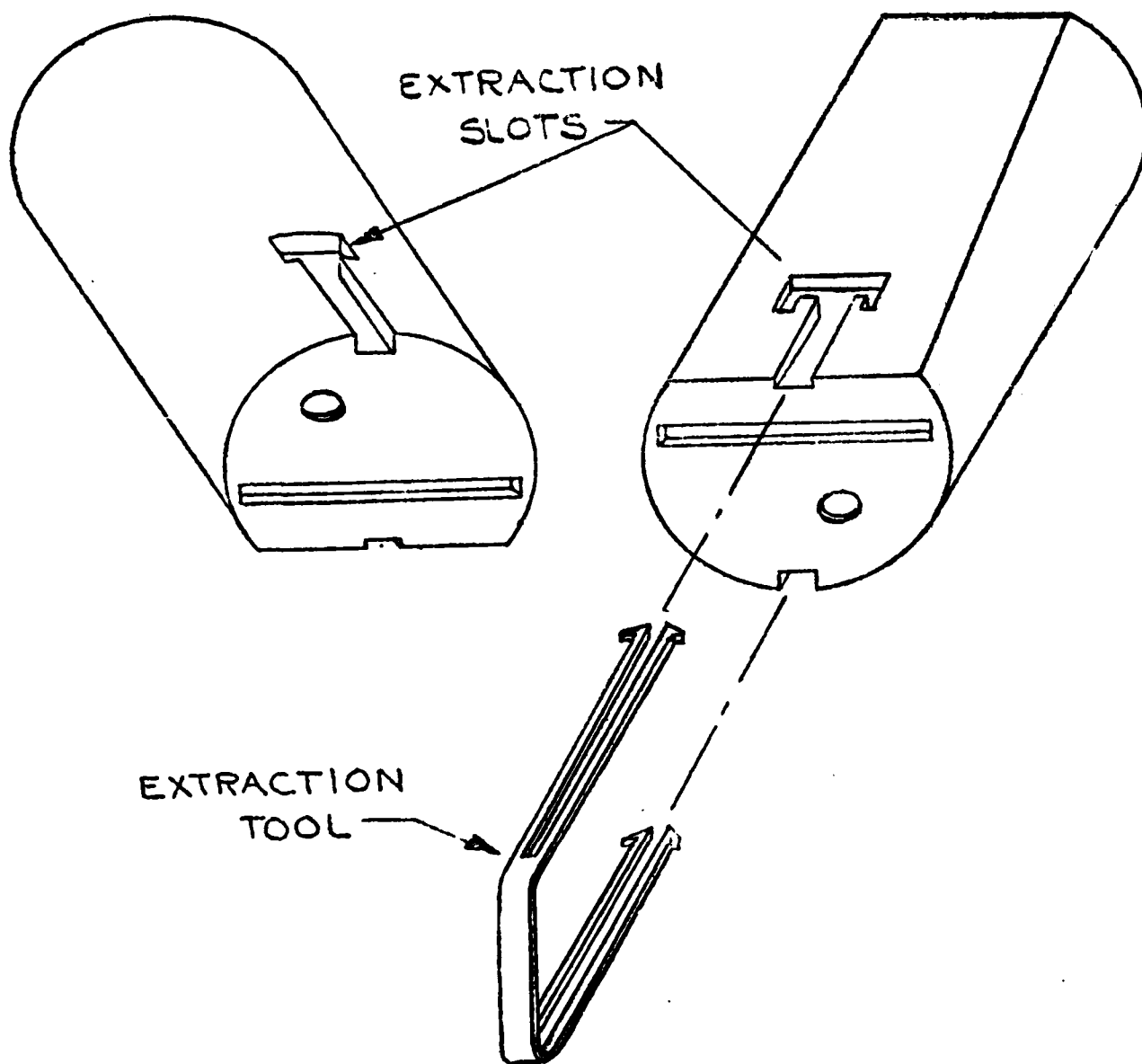


Figure 4.6 TCVCXO Extraction Tool

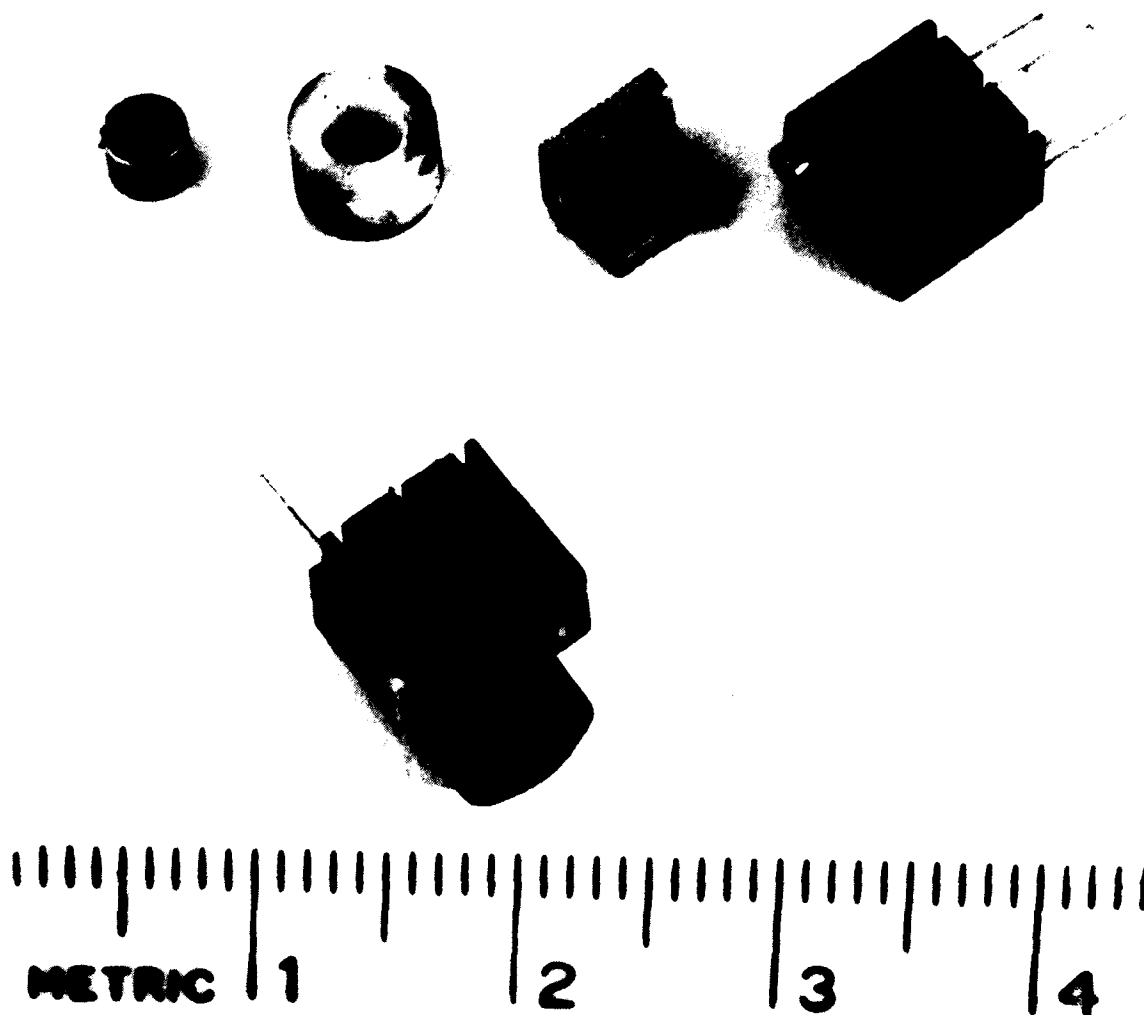
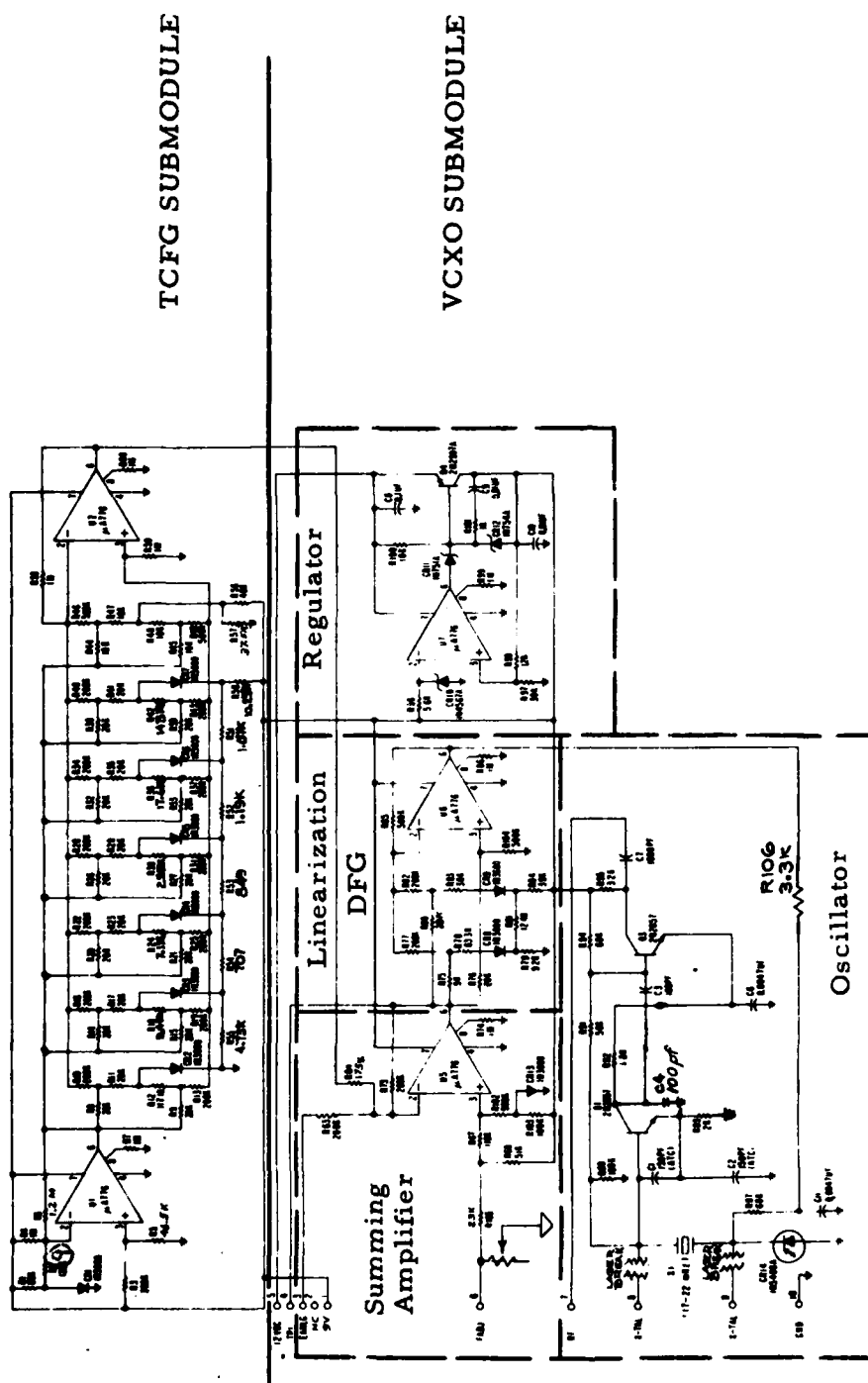


Figure 4.7 TCVCXO Exploded View, Potentiometer Assembly



### Figure 4.8 TCVCXO Circuit Partitioning

#### 4.3 Hybrid Microcircuit Construction

Each major part is fabricated as a separate hybrid microcircuit. Each hybrid consists of a 1.515" x 0.900" x 0.030" alumina substrate metallized with a thick-film conductor-resistor pattern. Integral crossover connections are achieved by means of thick-film dielectric material. Chip components attached to the metallized substrate complete the circuits. In the final version, the chip components consist of diodes and transistors in chip-and-wire form, integrated circuits in chip-and-wire form, and chip capacitors. In addition, the VCXO hybrid incorporates a crystal housed in a custom ceramic flatpack.

Table 4-1 gives the component count by generic type and the method of component assembly for each hybrid type in the final product.

Ultrasonic ball-bonded gold wire is used for the interconnection of all semiconductor chips. Gold wire was selected over aluminum because of the well-documented reliability problems associated with aluminum wire bonds on most thick-film gold materials. Ultrasonic ball bonding was selected over conventional thermocompression bonding to avoid exposure of the gold-wire-to-aluminum film interface on the chips to excessively high temperatures and an attendant "Purple Plague" intermetallic problem.

The selection of soldering and eutectic die bonding as the processes for attaching chip capacitors and semi-conductor dice, respectively, was made because the use of conductive epoxy was expressly prohibited on this program. The requirements of MIL-M-38510 have been followed throughout.

#### 4.4 Hybrid Construction and Layout Changes

During the course of the contract, both TCFG and VCXO modules underwent significant changes. The original manufacturing concept, applied to the first engineering samples, employed three resistor paste blends to manufacture all the resistors on the substrates. It was determined subsequently, however, that the

TABLE 4-1. COMPONENT COUNT AND ASSEMBLY

<u>Component</u>	<u>Assembly Method</u>	<u>Qty./Substrate Type</u>	
		<u>TC</u>	<u>VCXO</u>
Ceramic Porcelain Chip Capacitors	Soldering	—	8
		—	4
Bipolar IC Chips Transistor Chips Diode Chips	Eutectic Die Bonding	2	3
	& Ultrasonic (gold)	—	3
	Ball Bonding	7	7
Crystal (Ceramic Flatpack or HC18 to T05)	Epoxy to Mounting Strip, Solder to Circuit	—	1
TOTAL		9	26



use of four blends would provide better control of resistor values after firing and widen the trimming range, albeit at some sacrifice in manufacturing cost.

The original design concept suggested by ERADCOM mandated the use of beam lead devices in preference to chip-and-wire components wherever possible. This concept had to be abandoned for a variety of reasons. It was discovered early in the program that only two of the required device types were available in beam lead form. Although the original 100% goal was impossible, the hybrids were designed using the beam lead devices that were available. It was later decided that the continued usage of beam lead devices placed an unnecessary burden on hybrid manufacture with few resultant benefits. Additionally, a reliability consideration entered into this decision. Since solder must be used to attach capacitors onto the VCXO hybrid, the possibility of flux entrapment under beam lead devices exists, even though the hybrid assemblies were cleaned after capacitor attachment.

Layout changes were also dictated by problems encountered in passive trimming, component assembly, and active or functional trimming. Passive trimming showed that (1) a number of resistors were covered with corral glass and were, therefore, unstable and difficult to trim, and (2) some resistors had insufficient trim range because of the fabrication problem discussed above. The problems in component assembly resulted from the close proximity of wire bonds and components to the corral wall and indirectly from the high circuit density. The functional trimming problems indicated the need to increase the trim range of some resistors and to move others farther away from the corral.

The original VCXO layout (Figure 4.9) was based on ERADCOM's original specification and schematic (see Figure 4.10); hence the original VCXO layout included two integrated circuits which were subsequently eliminated (Figure 1.3) when Amendment 4 of SCS-483 revised the requirement for digital modulation. The original layout also included provisions for mounting the crystal within the corral; the change in scope which permitted the use of metal cased crystals also resulted in the removal of the crystal from the interior of the corral and freed additional area on the VCXO substrate.

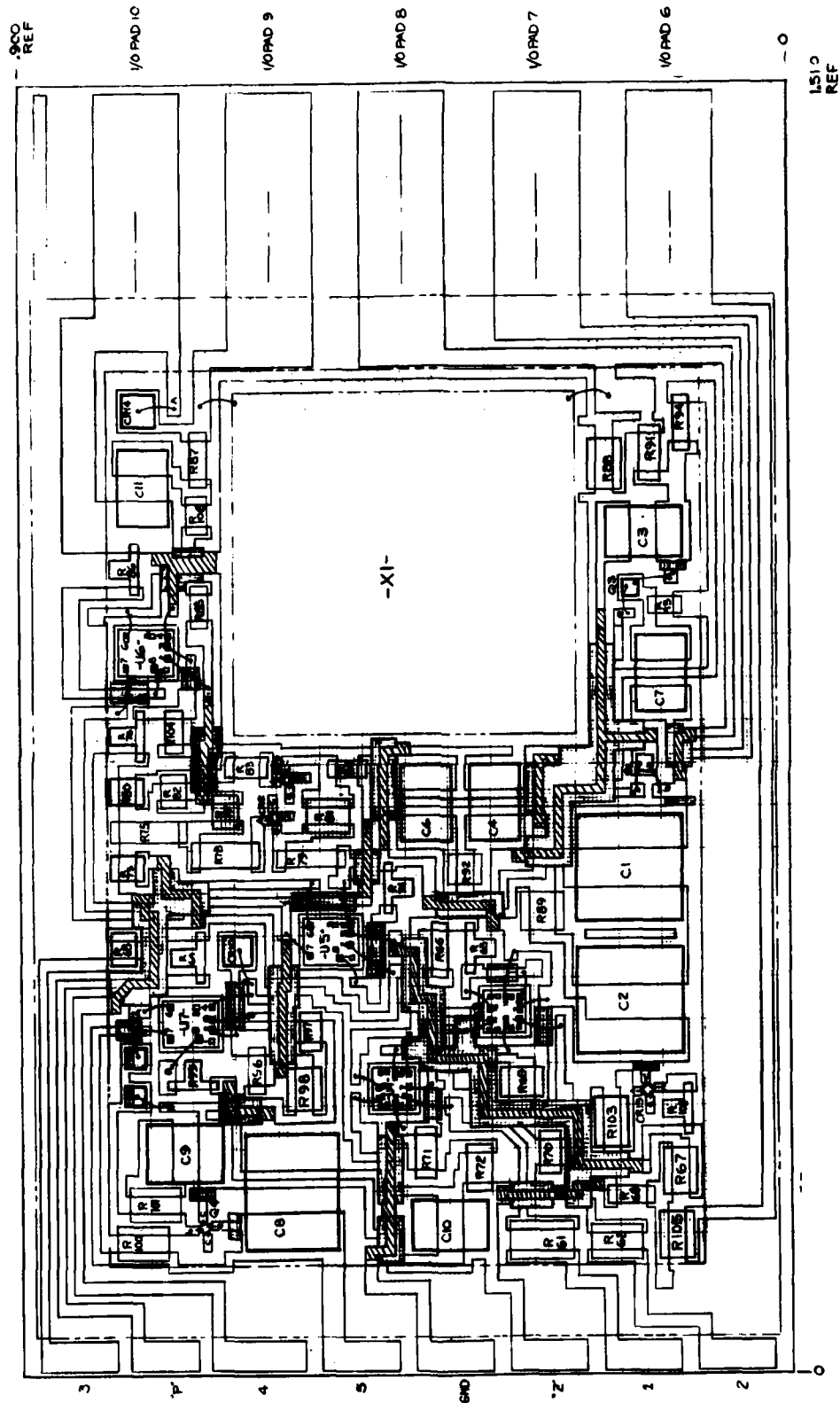


Figure 4.9 TCVCXO Original VCXO Layout

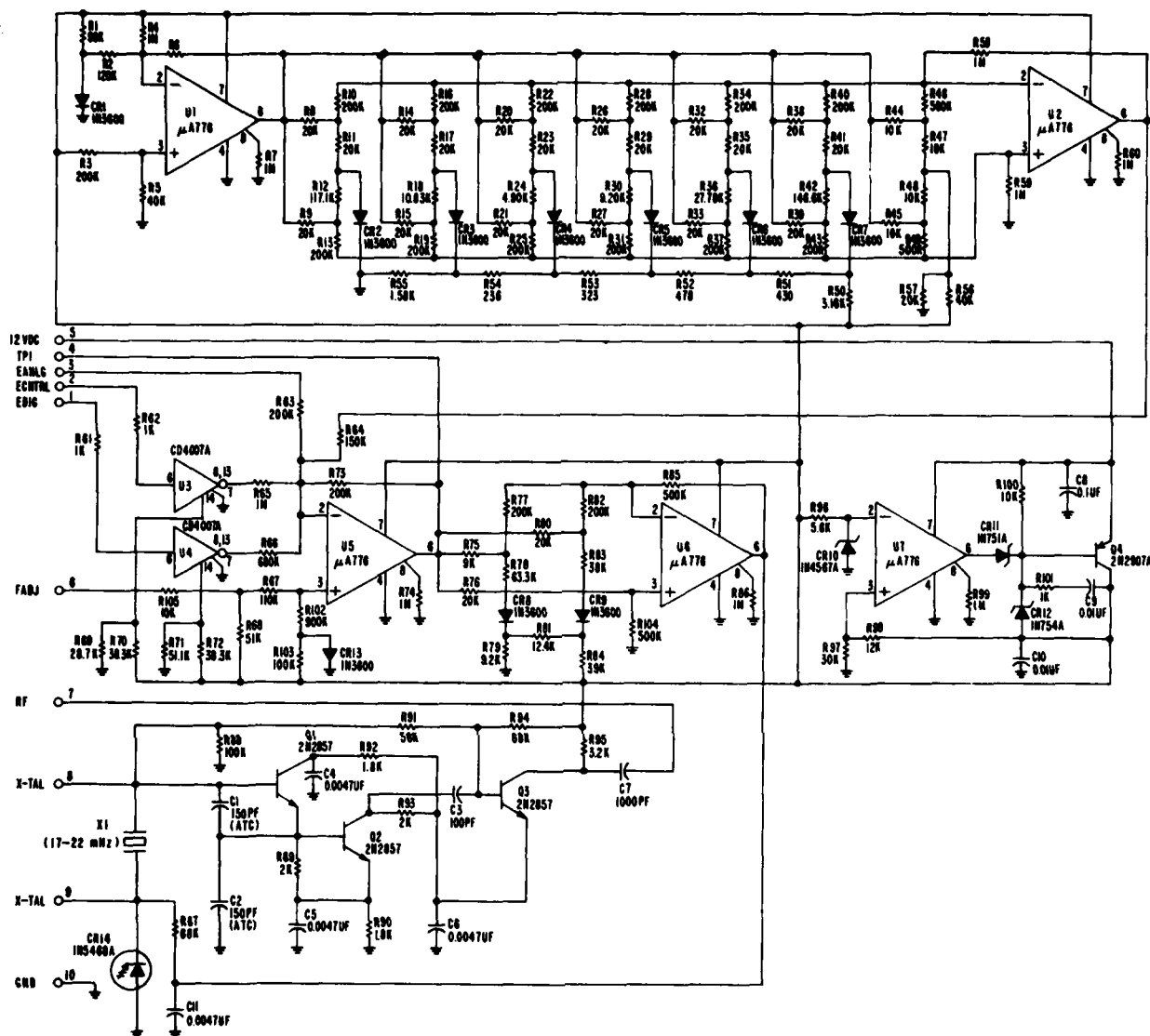


Figure 4.10 Original TCVCXO Schematic

The original VCXO layout employed large 150 pF porcelain capacitors for C1 and C2; cost and procurement considerations dictated the use of cheaper and thinner 75 pF units in parallel for the final version. The final version of the VCXO layout is shown in Figure 4.11.

The original TCFG layout (Figure 4.12) is compared with the final version (Figure 4.13) which incorporates the changes referenced above.

#### 4.5 Process Flow Plan

The final process flow charts for each of the submodules and for the TCVCXO module are presented in Figures 4.14, 4.15, and 4.16 (Raytheon Dwgs. D31363, D31364, and D31365). These drawings, and the pertinent Operation Standards referenced thereon, constitute Part 2 of this final report.

Figure 4.17 summarizes the overall manufacturing process, starting with the virgin substrates, their progress through the various manufacturing stages leading to the fabrication of the TCFG and VCXO submodules, and thence the marriage of the submodules to yield the final TCVCXO unit.

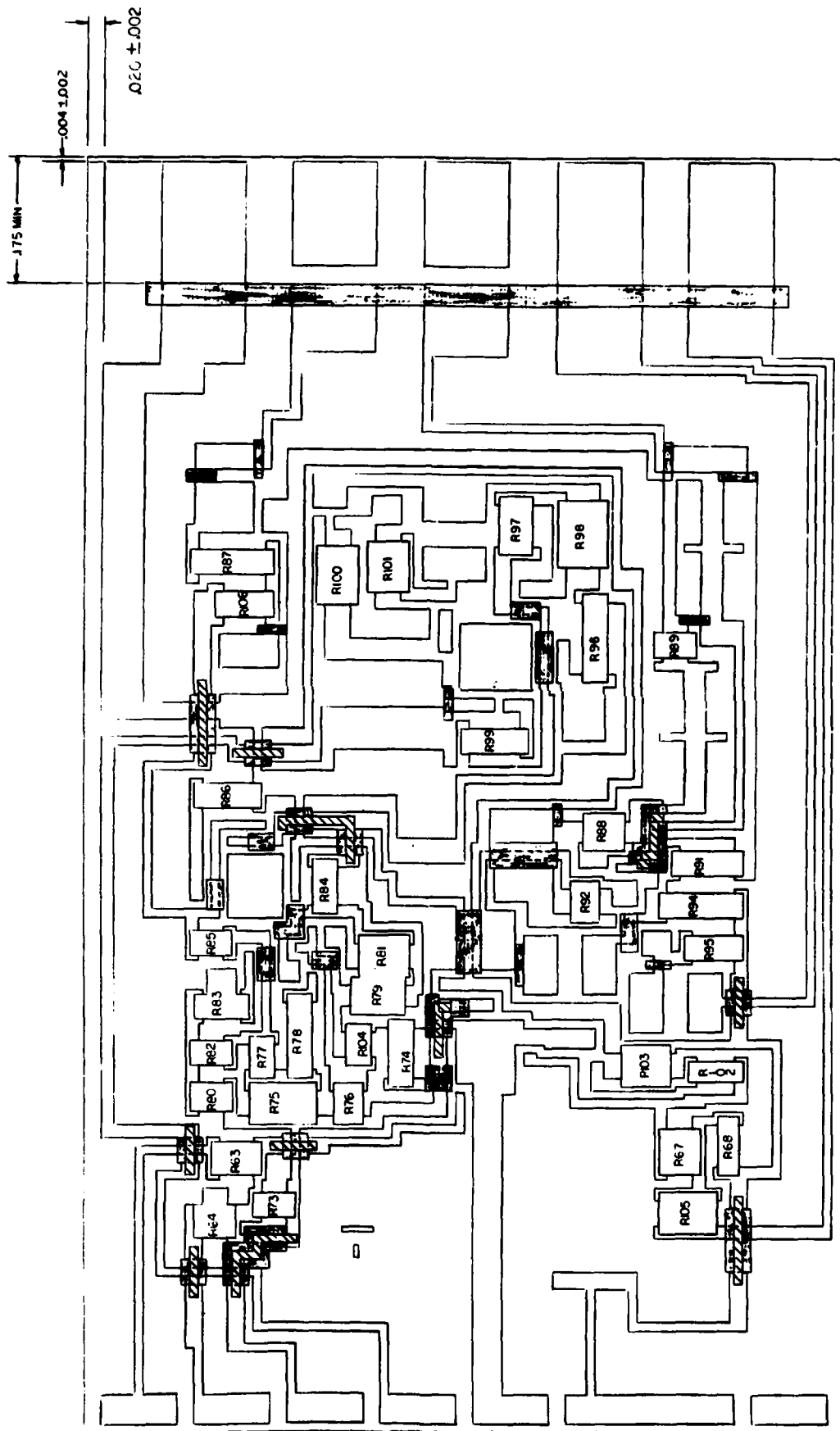


Figure 4.11 Final VCXO Layout

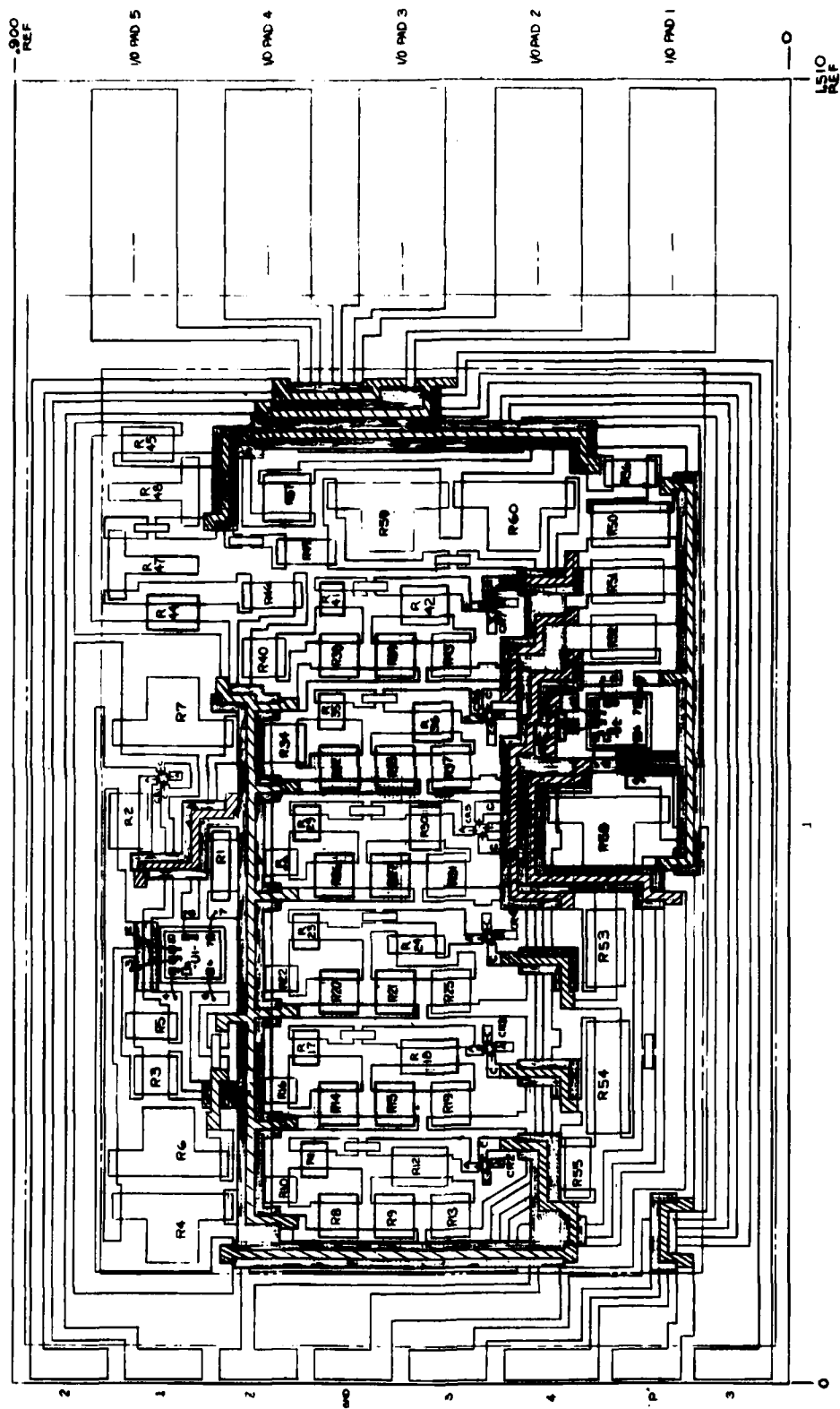


Figure 4.12 Original TCFG Layout

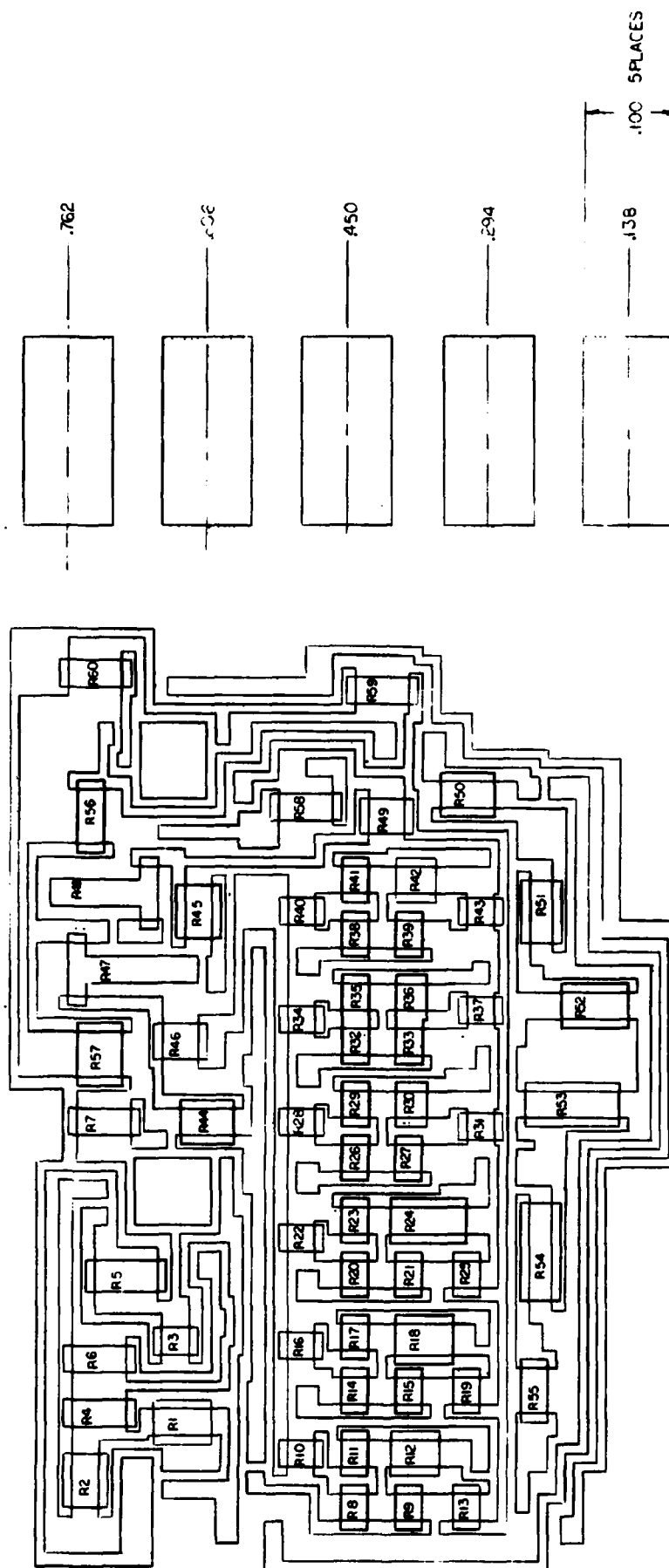


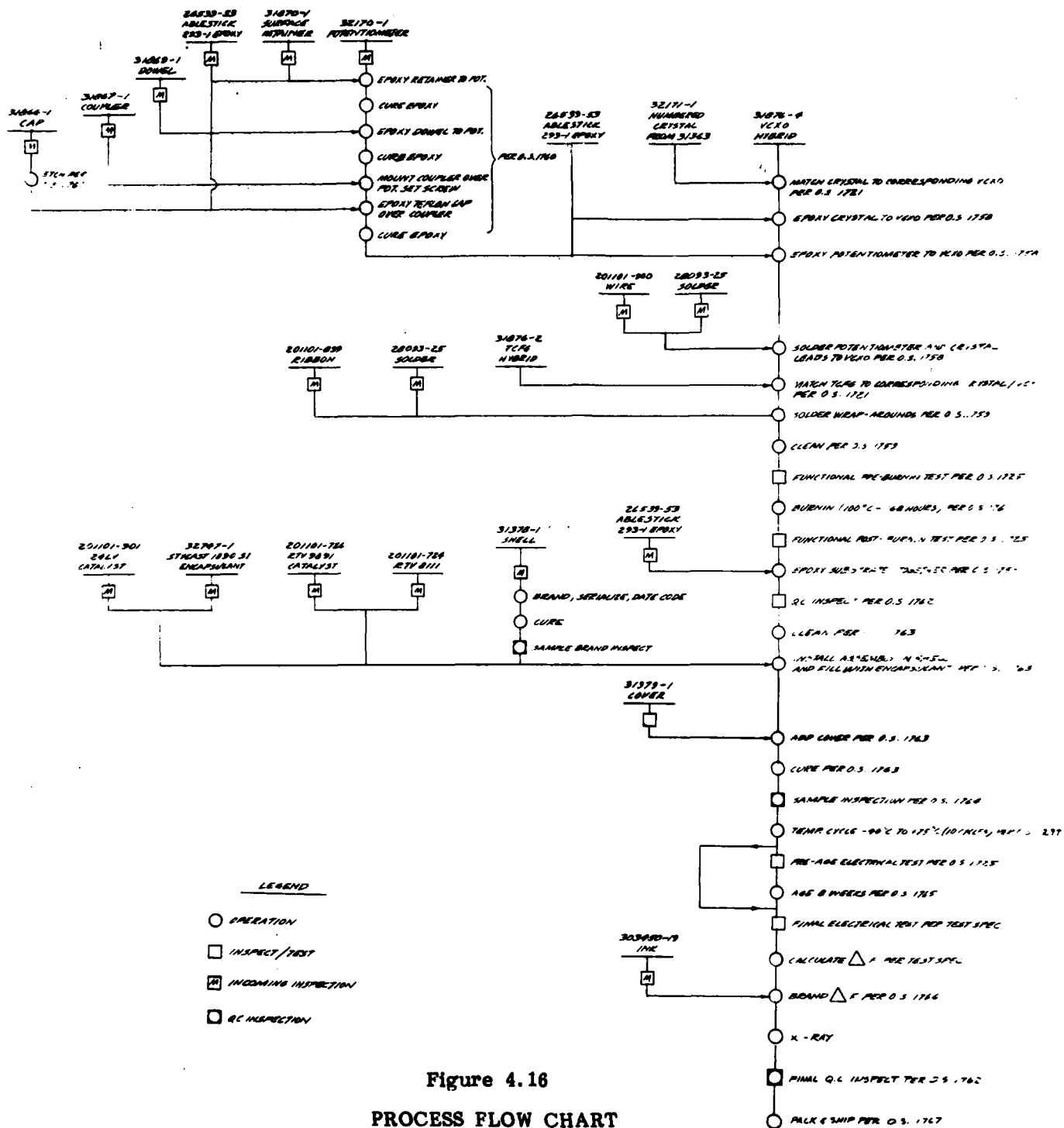
Figure 4.13 Final TCFG Layout







**Figure 4.15**  
**PROCESS FLOW CHART**  
**TCFG HYBRID**  
**(Raytheon Dwg. D-31364)**



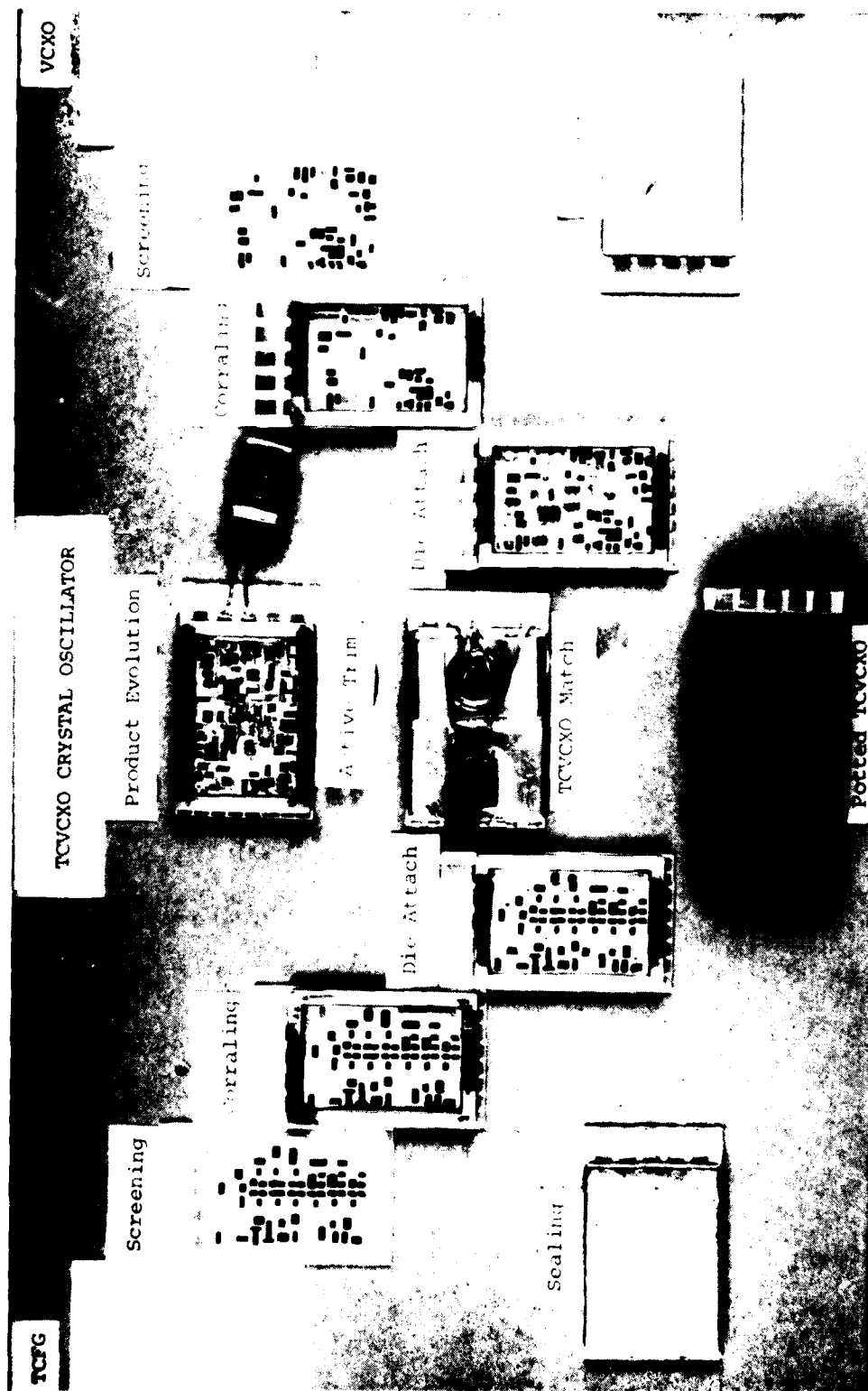


Figure 4.17 TCVCXO Process Sequence Summary

## 5.0 MANUFACTURING PROCESSES

### 5.1 Hybrid Technology

Hybrid thick-film technology is based on a manufacturing concept in which the majority of the passive components that constitute a functional electronic circuit, as well as their interconnections, are formed by a screen printing process rather than by soldering individual elements. The technique yields controllable, reproducible, essentially two-dimensional circuits capable of performing reliably over wide environmental conditions. High frequency capability, vital to oscillator performance, is made possible by the inherently low parasitic capacity and low dielectric loss characteristics of the materials used in thick-film hybrid construction. Design and production flexibility are guaranteed, since active devices produced by various semiconductor process technologies can be combined within a single hybrid circuit, and since the components formed by the screen printing process can be easily trimmed with a high degree of accuracy.

The base upon which the circuit is formed is termed a substrate. It provides physical support for the circuit, thermal transfer between components, and isolation between conductors. Substrates should be flat, reasonably smooth, chemically inert, mechanically strong, and capable of withstanding high temperature processes.

The design process, initially, involves the fabrication and testing of a functional breadboard. The transfer of the working circuit to hybrid microcircuit form involves considerations of final package size and configuration, power dissipation, film paste properties, and chip component geometries. Company design guidelines are generally available defining processes, component form factors, and crossover, land, and conductor dimensional constraints. Master drawings of conductor and resistor patterns are then made, and rubylith masters are derived from them. Those masters, in turn, are reduced photographically to the final circuit size, and the resulting photographic plates are used to photoetch stainless steel mesh screens through which the thick-film circuit will be printed onto the substrate.

The screening process involves forcing the conductive, resistive, and dielectric paste materials onto the substrate through a succession of screens which have been photo-etched to form the desired configuration. Perfect registration of the screens is essential to achieve the required final geometry. Inks or pastes for conductors and resistors are composed of precious or semiprecious metal powders combined with various organic and inorganic binders and solvents; physical, chemical, and rheological properties are rigorously controlled. Dielectric pastes are composed of suspensions of alumina, glass, and ceramic powders in suitable binders. After each screening, the substrate is fired by passage through a belt furnace under controlled temperature and cooling rate conditions. Conductors are usually screened and fired first, followed by dielectric layers (for cross-overs or for thick-film capacitors), then by resistors, and finally by a glaze coat. Successive firings are usually carried out at successively lower temperatures. After final firing, resistors are trimmed to the desired final value by a mass-removal process in which material is subtracted either by a sandblasting abrasive process or by a high-intensity laser beam. Measuring probes in contact with the substrate monitor the resistance value in process and terminate the trimming procedure when the desired component value has been reached. The TCVCXO uses laser trimming exclusively.

The next step involves the attachment of discrete components in chip form to the substrate, and their electrical connection to the circuit. Chip attachment is performed either by conventional soldering techniques, eutectic bonding, or with adhesives (conductive or non-conductive). Electrical connections are achieved through the techniques of thermocompression wedge and ball-wire bonding, ultrasonic bonding, or combinations of the three processes. In all cases, the object is to achieve intimate contact between the materials - the substrate conductors or the metallized lands on a semiconductor chip on the one hand, and the interconnecting wire (generally gold) on the other - to obtain an atomic interface at the connection. By ERADCOM directive, no adhesives are to be used in any internal circuit of the TCVCXO.

All manufacturing processes require a high level of cleanliness, and materials require a high degree of purity and constant monitoring to ensure conformance with the required standards. Quality Control procedures for the final products, in addition

to standard electrical tests, include special burn-in processes to ensure stability and long life, and special mechanical and visual inspection schemes to determine proper wire bond formation, reliable adhesion of materials to the substrate, and adequate chip component attachment. Final packaging of the working substrates in conformance with specific requirements completes the assembly process.

## 5.2 Substrates

Both TCFG and VCXO circuits employ the same alumina substrate. Size is 1.515 x 0.900 x 0.030 inches.

## 5.3 Artwork Generation

The master artwork for the thick-film patterns to be screened onto the ceramic substrates was machine-generated at Raytheon's automated drafting center. The procedure initially involved preparing "digitizable" layout drawings showing line widths and routings symbolically. The design information on the color-coded digitizable drawings was then transferred, through man-machine interface, onto magnetic tape which was then used to drive a photo-plotter. Artwork was photoplotted on film at 5X or 20X scale for each of the thick-film conductor, resistor, and dielectric insulator patterns constituting the designs. Design guidelines for the circuits were based on Raytheon Operation Standard 1585, "Design Practices for Hybrid Circuit Layouts". Special attention was paid to resistor location and configurations to facilitate laser trimming. For each hybrid submodule, eight sheets of artwork were generated as follows:

- Sheet 1 - First conductor
- Sheet 2 - Dielectric insulator
- Sheet 3 - First conductor overlay
- Sheet 4 - Second (crossover) conductor
- Sheet 5 - Resistor, 2K  $\Omega/\square$
- Sheet 6 - Resistor, 20K  $\Omega/\square$
- Sheet 7 - Resistor, 200K  $\Omega/\square$
- Sheet 8 - Resistor, 500K  $\Omega/\square$

Screening layouts for both VCXO and TCFG submodules appear on Figures 5.1 to 5.11.

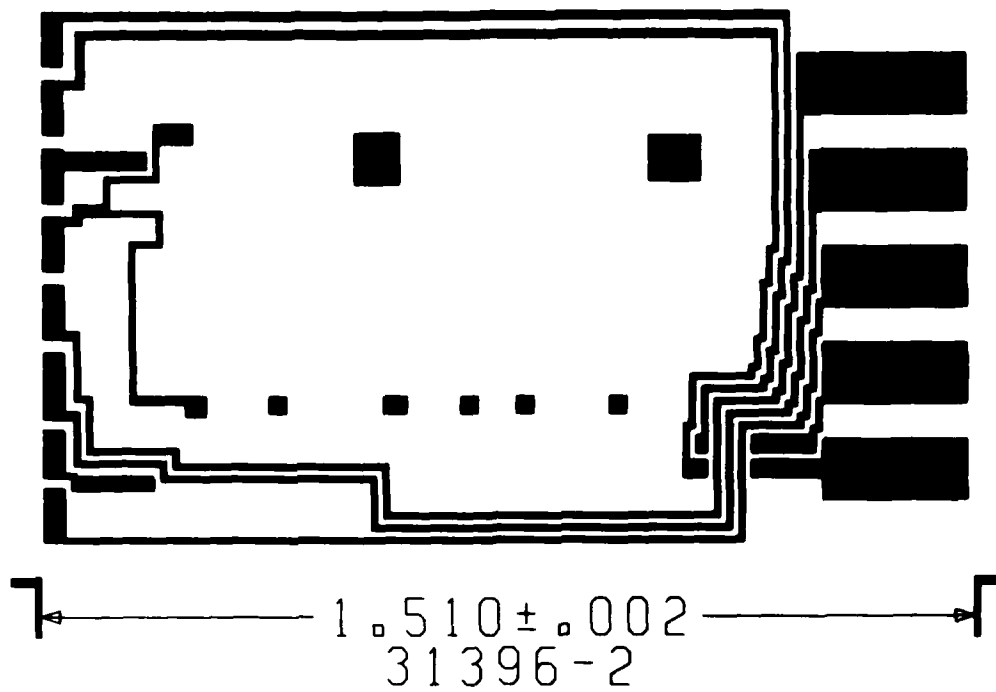


Figure 5.1A Screen TCFG First Conductor

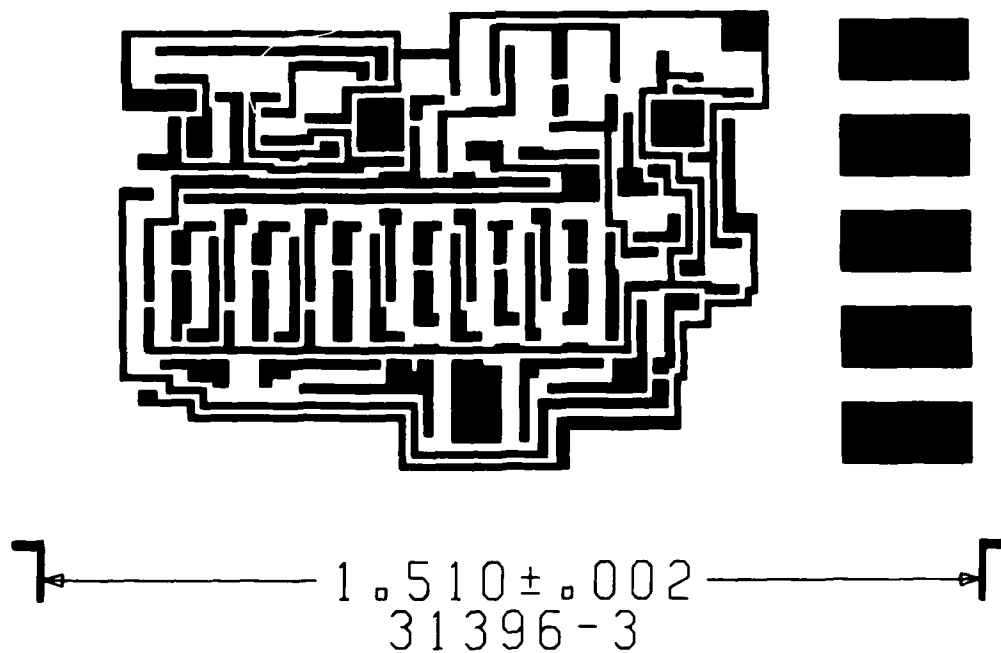


Figure 5.1B Screen TCFG Second Conductor

T1

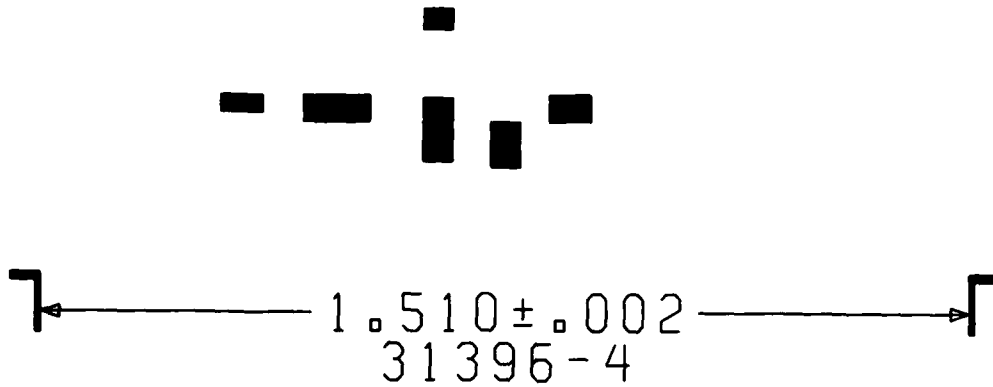


Figure 5.2A Screen TCFG First Resistor

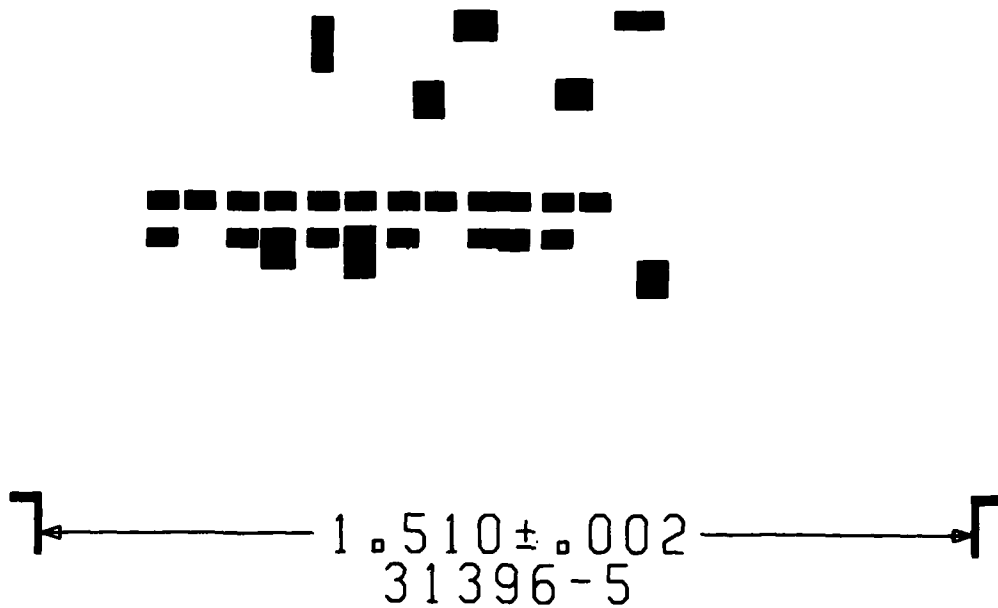
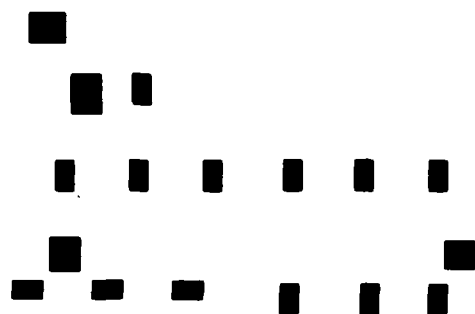


Figure 5.2B Screen TCFG Second Resistor








 $1.510 \pm .002$ 
  
 31396-6

Figure 5.2C Screen TCFG Third Resistor






 $1.510 \pm .002$ 
  
 31396-7

Figure 5.2D Screen TCFG Fourth Resistor

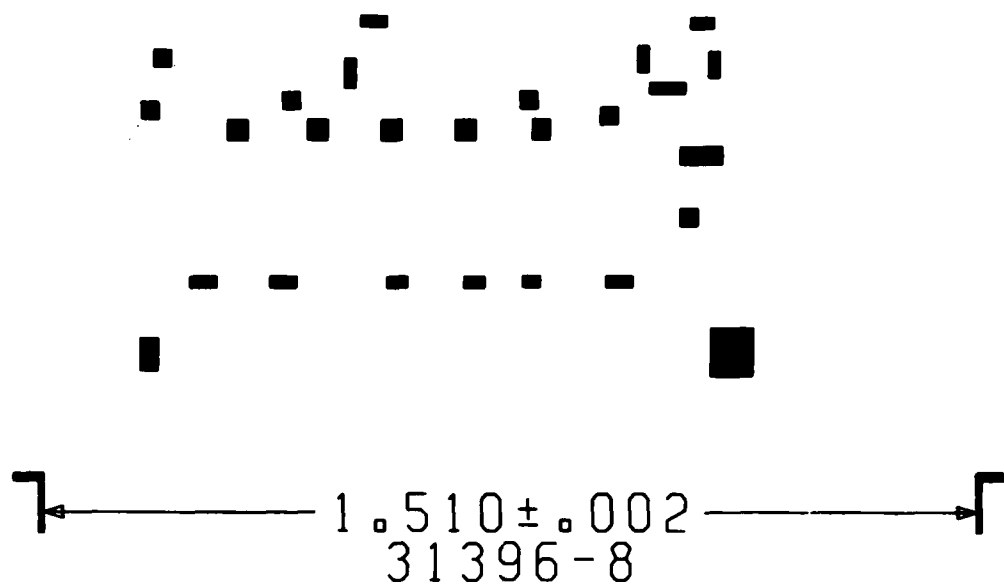


Figure 5.3 Screen TCFG Dielectric

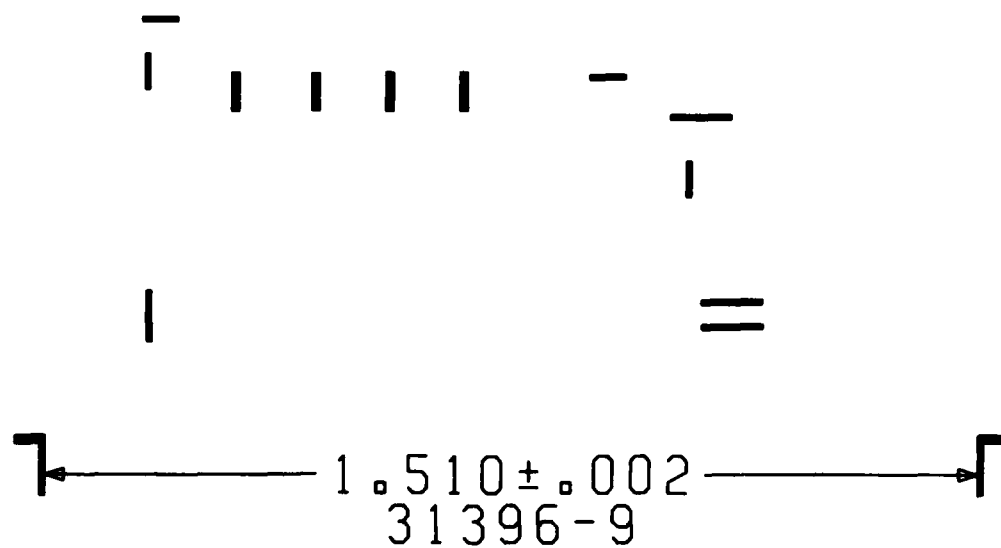


Figure 5.4 Screen TCFG Crossovers

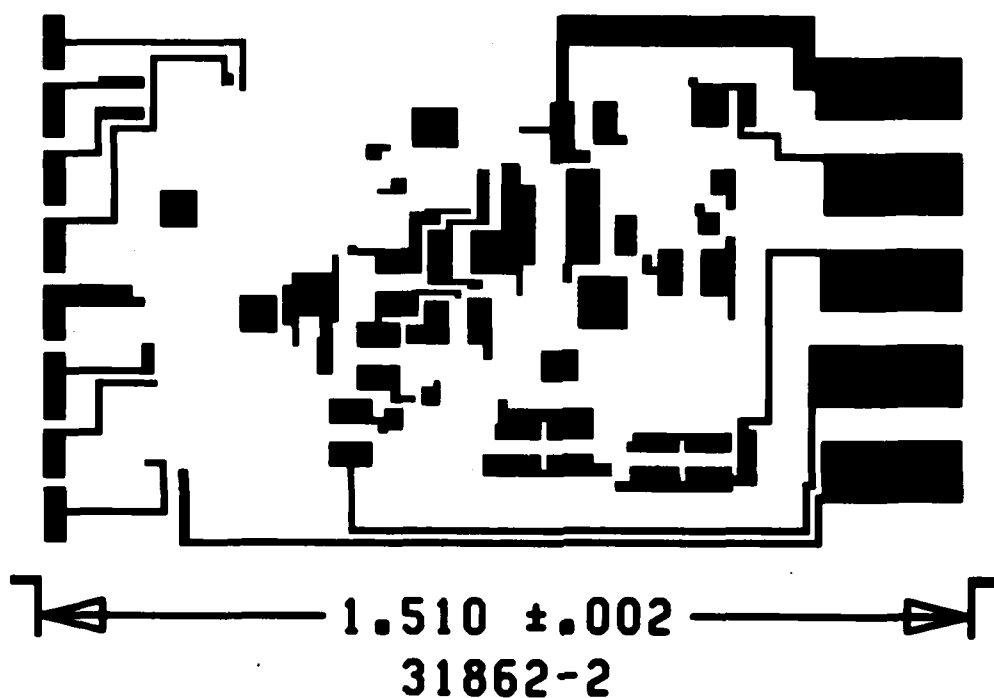


Figure 5.5A Screen VCXO First Conductor

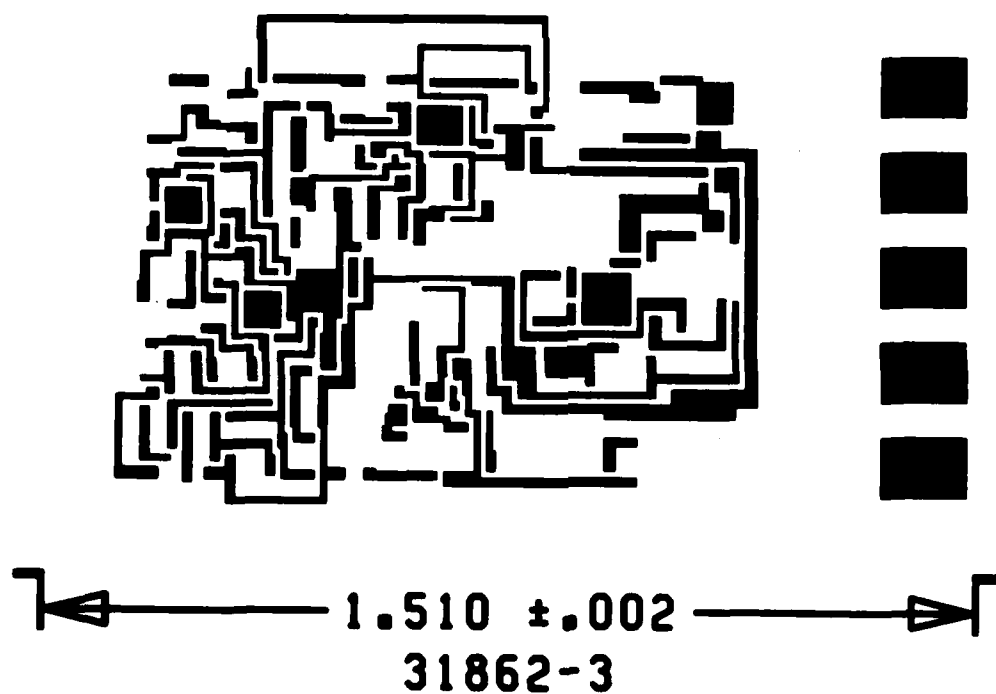


Figure 5.5B Screen VCXO Second Conductor

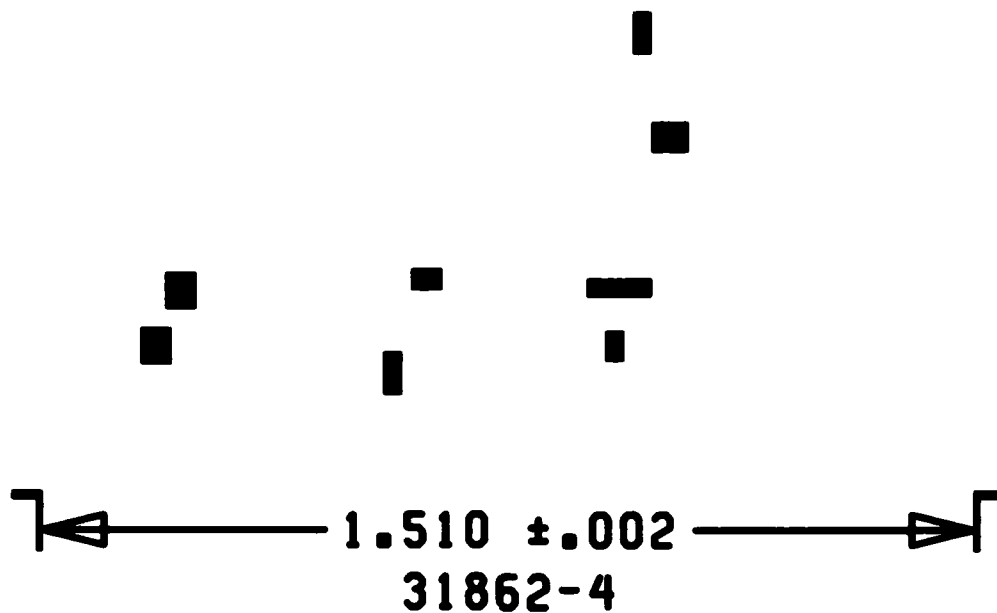


Figure 5.6 Screen VCXO First Resistor

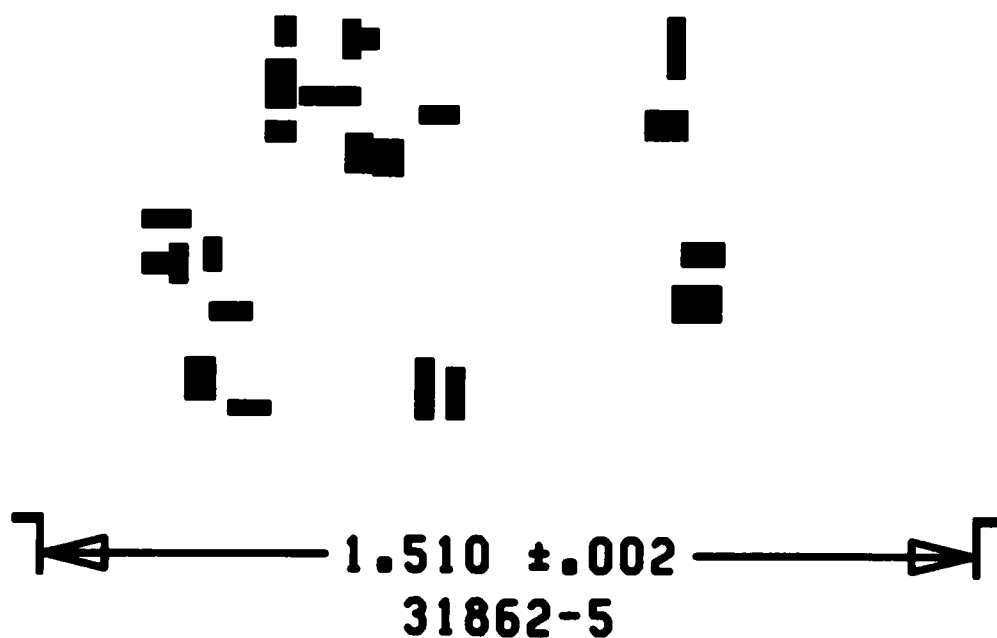


Figure 5.7 Screen VCXO Second Resistor

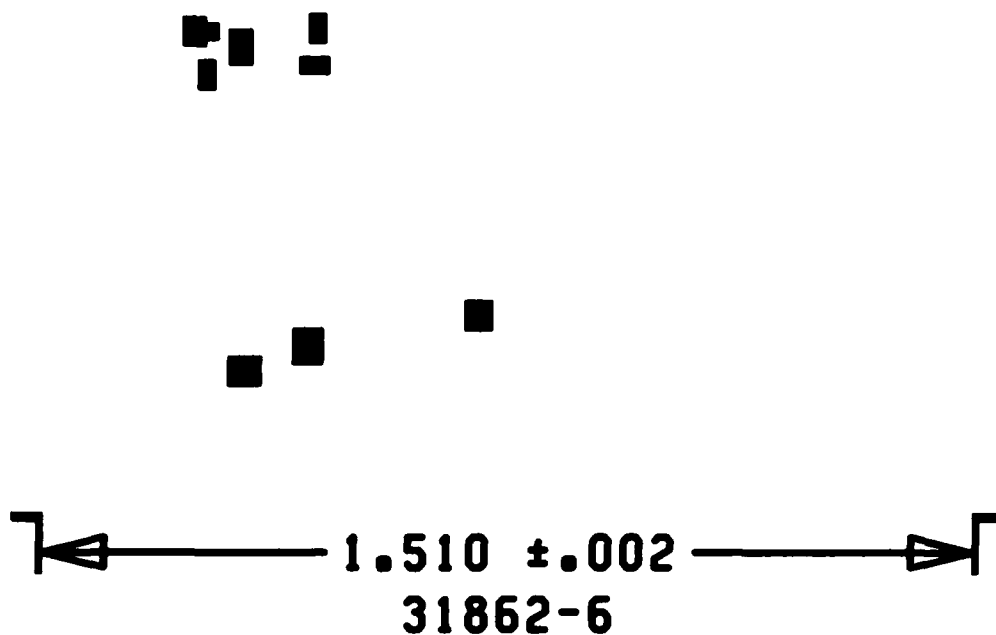


Figure 5.8 Screen VCXO Third Resistor

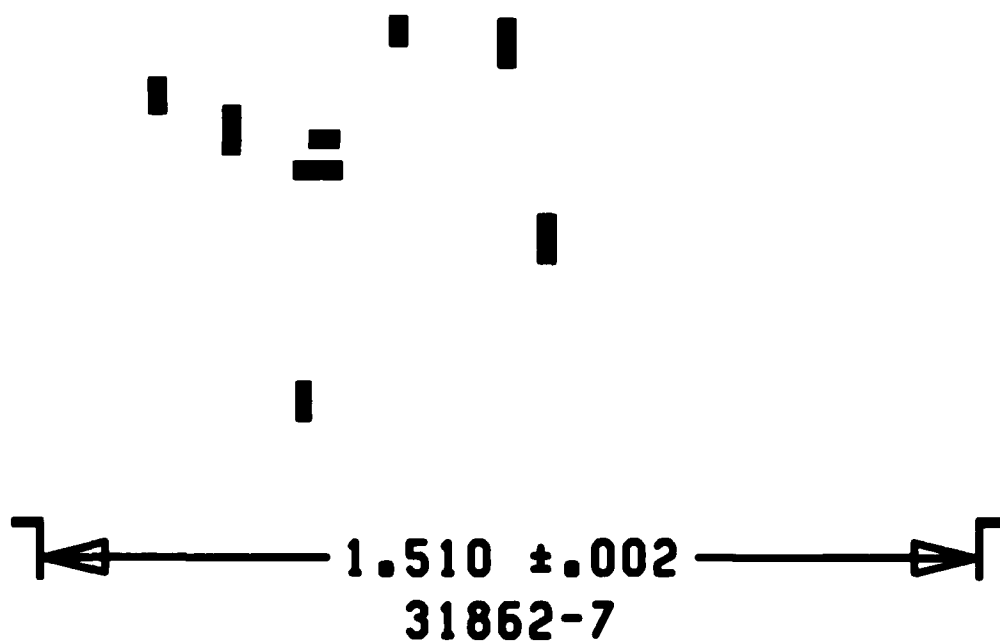


Figure 5.9 Screen VCXO Fourth Resistor

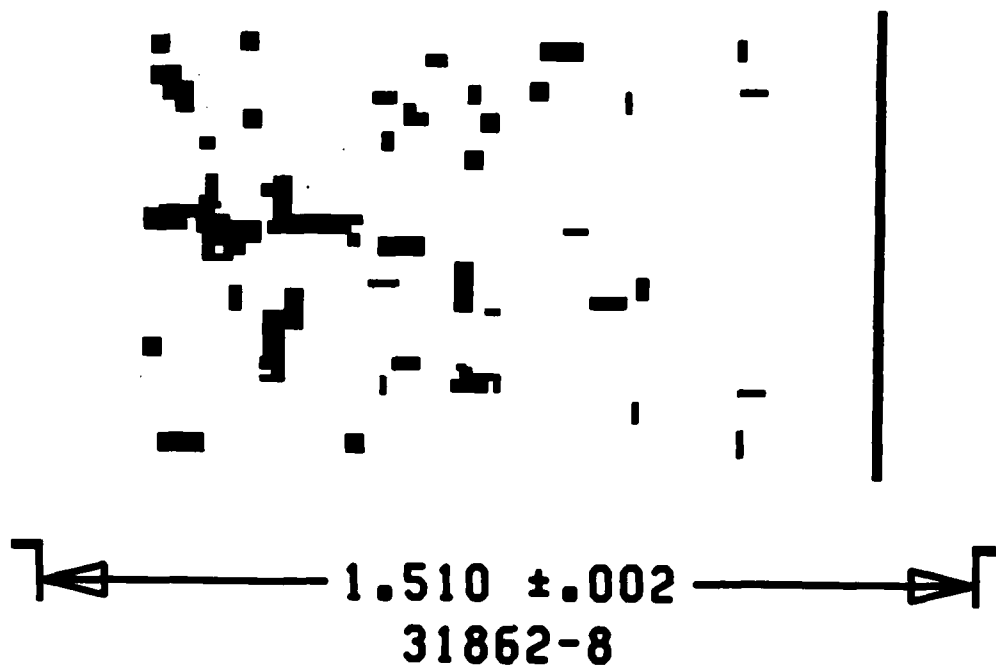


Figure 5.10 Screen VCXO, Dielectric

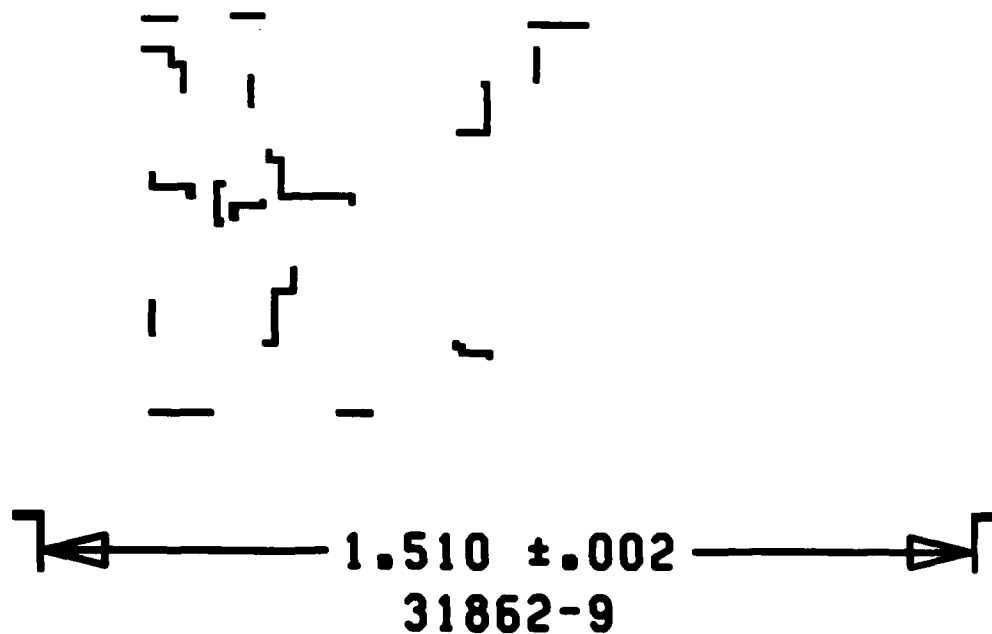


Figure 5.11 Screen VCXO, Crossover

#### 5.4 Screening

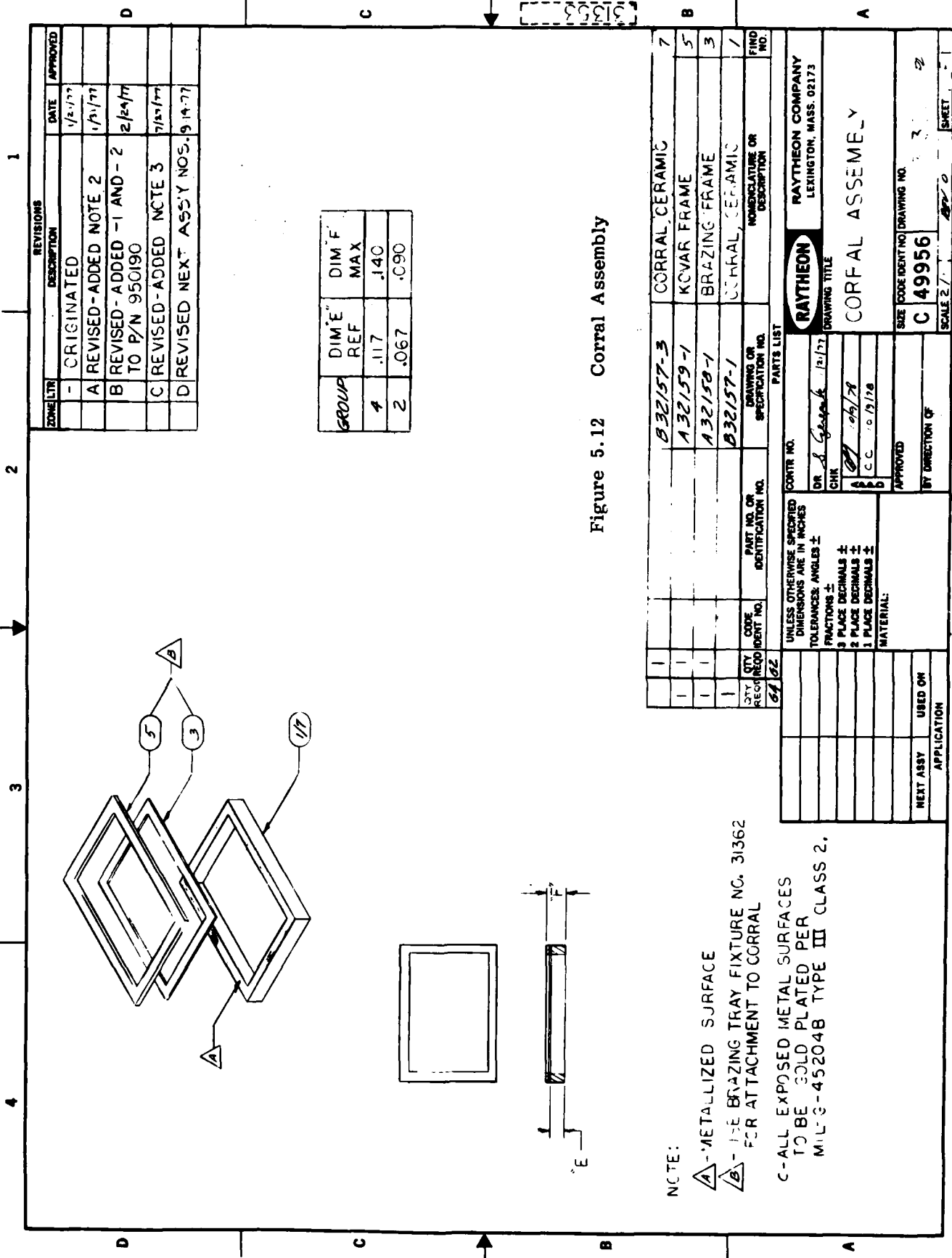
The circuitry is applied to the substrate through a total of eight screens: two conductors, four resistor pastes, one dielectric, and one for crossovers.

Screens are 325 mesh stainless steel mounted in aluminum frames. Screening is performed on a semi-automatic screen printer (Aremco Products Model 320). Four resistor paste formulations (500K ohms, 200K ohms, 20K ohms, 2K ohms) are employed; one conductor layer uses a gold paste, the other platinum gold. The latter is employed in those circuit areas to which soldered connections will ultimately be made. Firing is carried out in a tunnel furnace (Lindberg Model 47-HL-4361), reprogrammed as needed for each firing cycle.

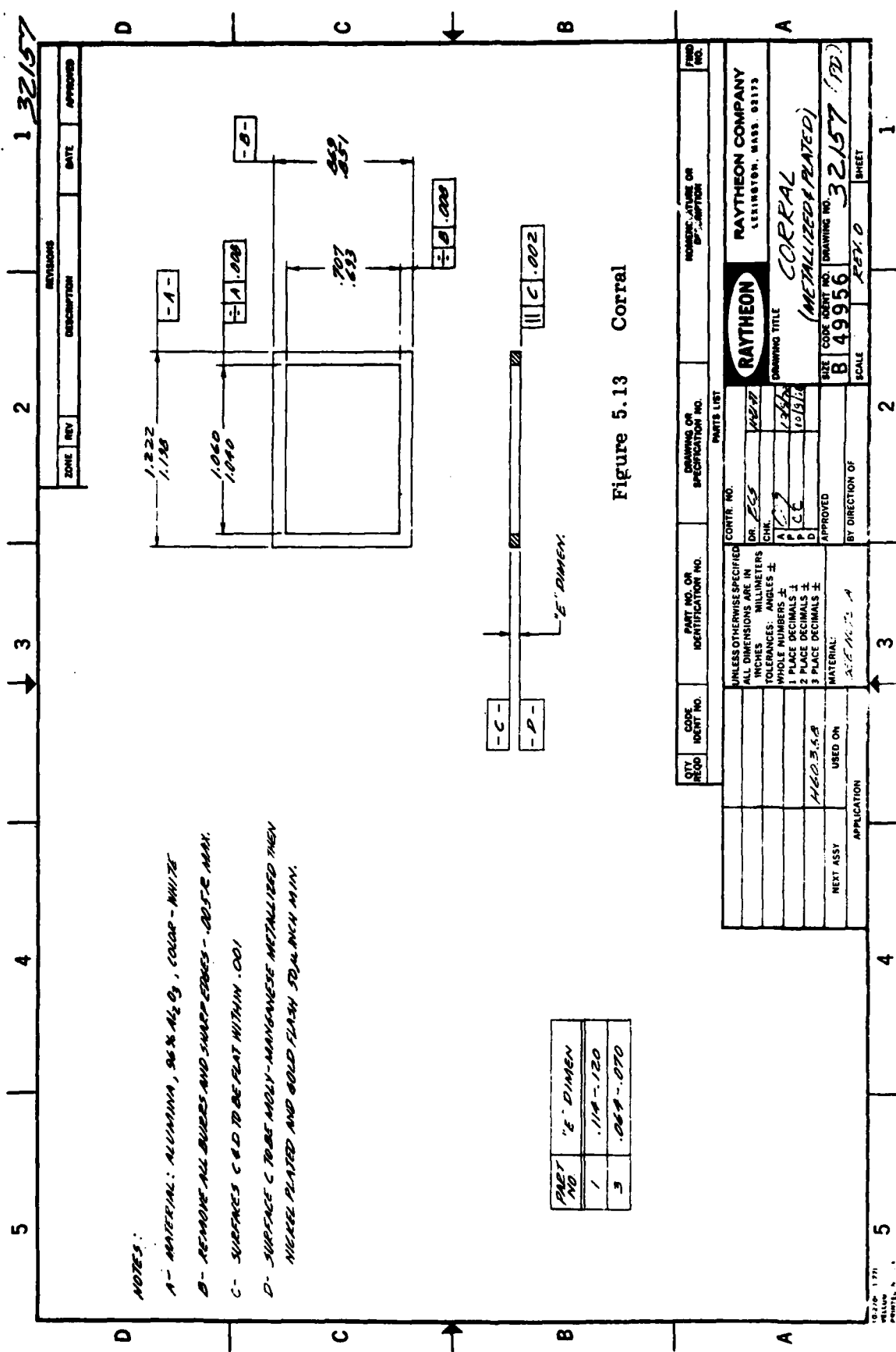
#### 5.5 Corral Assembly

Hermetic sealing of the submodules is accomplished through the use of a lidded corral enclosure fitted over the active circuit areas of the substrates. The process entails the fabrication of a frame or corral assembly, glass-sealing the corral assembly to the thick-film substrate, and, finally, parallel-seam-welding a flat metal cover to the top of the corral assembly. Fabrication of the corral assembly involves brazing a metal frame to a metallized alumina corral to facilitate, ultimately, the welding of a metal cover to achieve the final seal. After brazing, the exposed metal surfaces of the assembly are gold-plated to prevent oxidation during the glass sealing process. The corral assembly is pictured in Figure 5.12; materials and dimensional specifications for the ceramic corral, metal frame, and brazing alloy preform are described in Figures 5.13, 5.14, and 5.15. As previously stated, the corral assemblies for both submodules have the same cross-sectional dimensions, but different heights; hence, the metal frame and brazing frame are common to both units.

The ceramic corral frames were manufactured by dry-pressing, and purchased to dimensional tolerances of  $\pm 1\%$ . The tight tolerancing was required to allow for accurate fixturing of the final assembly, and did not create any serious procurement problem, as evidenced by the fact that 80% of the parts received exhibited variations







NOTES:

- A- MATERIAL: ALUMINUM, 96% AL<sub>2</sub>O<sub>3</sub>, COLOR - WHITE
- B- REMOVE ALL BUBBLES AND SHARP EDGES - .005" MAX.
- C- SURFACES C & D TO BE FLAT WITHIN .001
- D- SURFACE C TO BE MOLY-MANGANESE METALLIZED THEN NICKEL PLATED AND GOLD FLASH 50 μ INCH MIN.

Figure 5.13 Corral

QTY. REQD.	CODE IDENT NO.	PART NO. OR IDENTIFICATION NO.	DRAWING OR SPECIFICATION NO.	NAME, TITLE OR DESCRIPTION	FIG. NO.
				RAYTHEON COMPANY LEXINGTON, MASS. 02173	
PARTS LIST					
UNLESS OTHERWISE SPECIFIED					
ALL DIMENSIONS ARE IN INCHES: MILLIMETERS					
TOLERANCES: MILLIMETERS ±					
WHOLE NUMBERS ±					
1 PLACE DECIMALS ±					
2 PLACE DECIMALS ±					
3 PLACE DECIMALS ±					
MATERIAL: ALUMINUM					
NEXT ASSY USED ON					
APPLICATION					
CONTR. NO. DR. DES. CHK. DATE					
APPROVED BY: [Signature]					
RAYTHEON DRAWING TITLE: CORRAL (METALLIZED & PLATED)					
SIZE: CODE IDENT NO. DRAWING NO. 32157 (D)					
SCALE: REV. 0 SHEET 1					

APPLICATION			REVISIONS				
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED		
<i>H60388</i>							
<p><b>NOTES:</b></p> <p>A- PLATING: NONE</p> <p>B- SURFACES C &amp; D TO BE FLAT WITHIN .001</p> <p>C- TEMPER: ANNEALED</p>							
REV STATUS OF SHEETS		REV LTR				SPECIFICATION CONTROL DRAWING	
		SHEET NO.					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES  TOLERANCES: ANGLES $\pm$ FRACTIONS $\pm$ 3 PLACE DECIMALS $\pm .005$ 2 PLACE DECIMALS $\pm$ 1 PLACE DECIMALS $\pm$			CONTR NO. DR <i>ELC</i> 11-21-77 CHK APP <i>CC</i> 10/3/78 P <i>CC</i> 10/3/78 D APPROVED BY DIRECTION OF		<div style="text-align: center;"> <b>RAYTHEON</b> </div> <div style="text-align: center;"> <b>RAYTHEON COMPANY</b>            LEXINGTON, MASS. 02173         </div>		
MATERIAL: <i>.013-.017 THK. KOVAR</i>			DRAWING TITLE <div style="text-align: center; font-size: 1.2em;"> <i>KOVAR FRAME</i> </div>				
			SIZE	CODE IDENT NO.	DRAWING NO.		
			A	49956	32159 (FL)		
			SCALE 5X	REV. 0	SHEET		

10-2736 (6-72) VELLUM PRINTED IN U.S.A.

Figure 5.14 Kovar Frame

APPLICATION			REVISIONS				
NEXT ASSY	USED ON	LTR	DESCRIPTION		DATE	APPROVED	
			- A -				
			A .005 TOTAL		- B -		
			.700		.860		
			B .005 TOTAL				
<p><b>NOTES:</b></p> <p>A - MATERIAL: .003 THK. CUSIL, 72% SILVER, 28% COPPER PER ASTM - AWS BA<sub>9</sub>-B OR EQUIV.</p>							
REV STATUS OF SHEETS		REV LTR				SPECIFICATION CONTROL DRAWING	
		SHEET NO.					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES  TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± .005 2 PLACE DECIMALS ± 1 PLACE DECIMALS ±  MATERIAL:		CONTR NO.		<div style="border: 2px solid black; border-radius: 50%; padding: 5px; display: inline-block;">RAYTHEON</div>		<b>RAYTHEON COMPANY</b> LEXINGTON, MASS. 02173	
		DR <i>B63</i>					
		CHK		10/9/78		DRAWING TITLE  <div style="font-size: 1.5em; font-family: cursive;">BRAZING FRAME</div>	
		A P P D		10/9/78			
APPROVED		SIZE		CODE IDENT NO.		DRAWING NO.	
BY DIRECTION OF		A		49956		32158 (PD)	
		SCALE		REV. C		SHEET	
		5X					

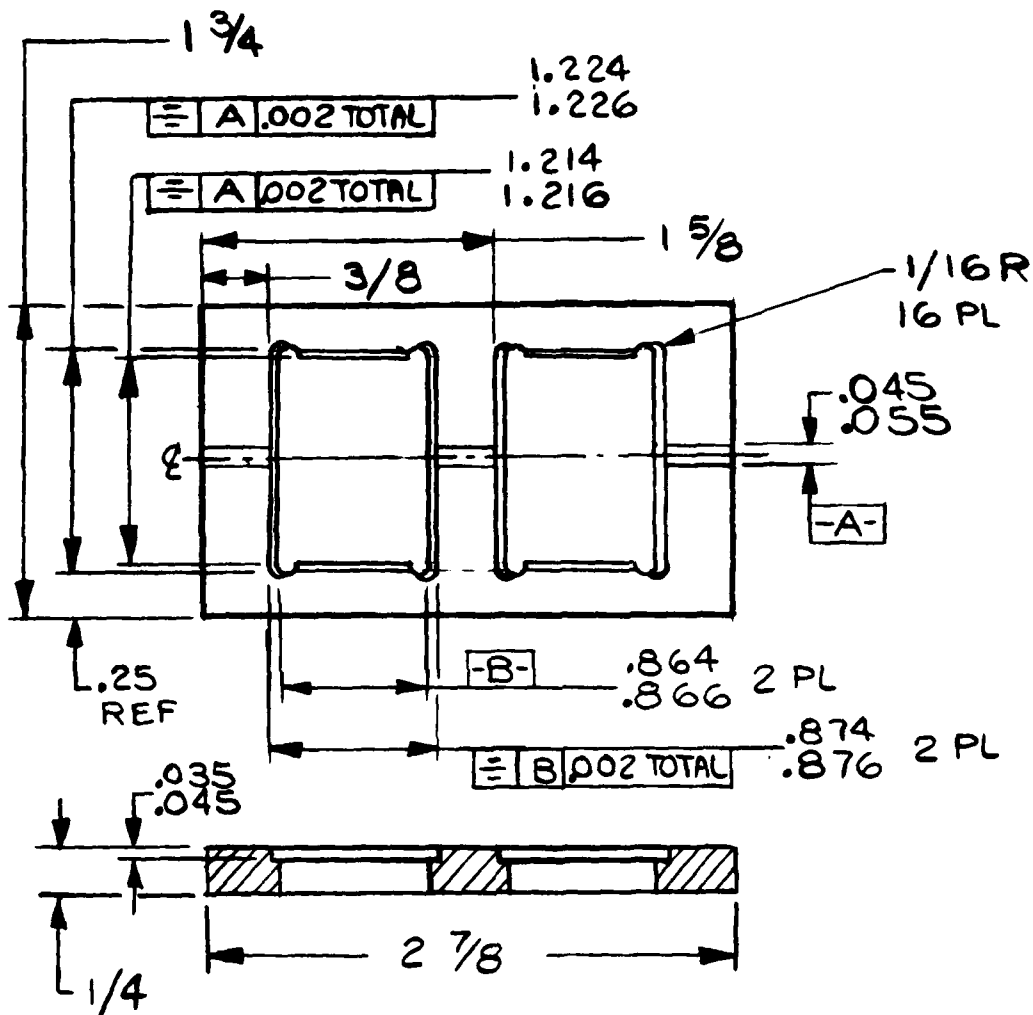
10-2736 (6-72) VELLUM PRINTED IN U.S.A.

Figure 5.15 Brazing Alloy Preform

of less than 0.5% for outside dimensions. Brazing preforms were etched from copper-silver eutectic sheet stock. Several fixtures were designed and built to locate the preform and frame properly with respect to the ceramic corral during the brazing process. The final process employs carbon fixtures which reference to the outside dimensions of the frame components.

The carbon brazing tray is shown in Figure 5.16; since the grade of carbon used has an expansion coefficient very similar to that of the kovar frame and the alumina corral, the fixture clearances can be designed for parts based on their room-temperature dimensions.

To attach the corral assembly to the thick-film substrate, the ceramic bottom surface of the corral assembly is first glassivated, using a tape transfer process to affix a glass preform; the glassivated assembly is then sintered in a furnace at about 500°C, thus fusing the glass to the ceramic. The glass is a modified lead-zinc borate devitrifiable solder glass with a thermal expansion coefficient reasonably well matched to that of alumina. Because of the tight tolerances required in the TCVCXO, it was necessary to design and fabricate a corral-substrate fixture to hold parts in accurate alignment during the bonding process. The fixture, after loading, is run through a belt furnace where the glass bonding agent is melted and the corral becomes firmly attached to the substrate. The fixture is illustrated in Figure 5.17 which depicts (a) the fixture base plate which incorporates three accurately spaced locating pins, (b) the parts of the fixture: from top to bottom, the base plate, the substrate retainer, and the corral positioner and retainer surrounding the weight, (c) the substrate and corral nested in the fixture, and (d) the fixture ready for the furnace, with the weight in place to provide the necessary pressure between the substrate and the corral. The furnace is programmed to provide a high rate of temperature rise to obtain low glass viscosity and good flow prior to devitrification. Figure 5.18 shows the complete substrate-corral assembly.

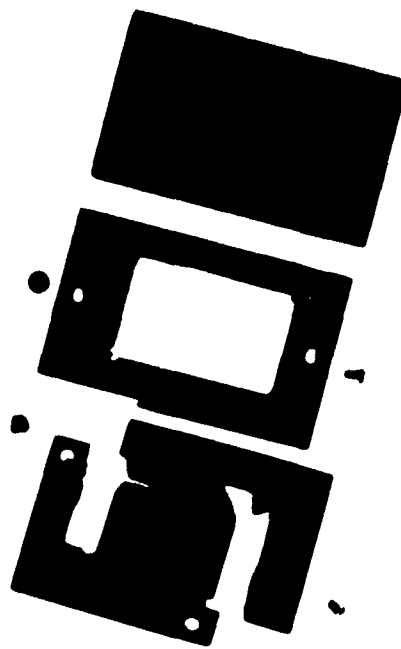


NOTES  
 1. MATL: W-120 (L-56) CARBON  
 2. TOL: FRACTIONS  $\pm \frac{1}{32}$

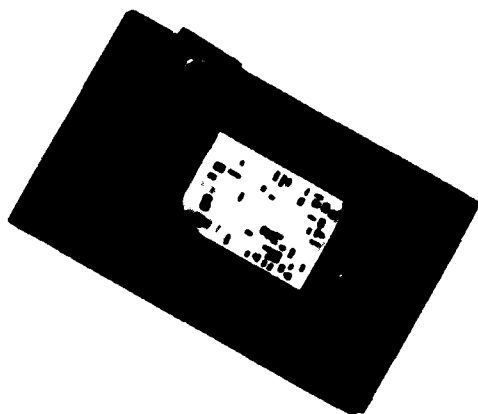
Figure 5.16 Carbon Brazing Tray



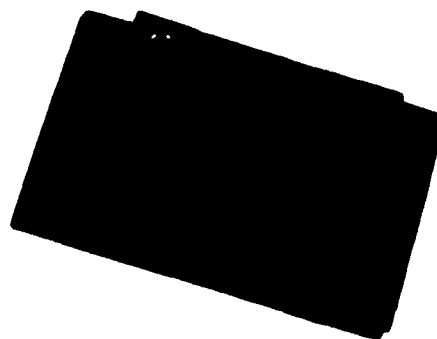
(a)



(b)



(c)



(d)

Figure 5.17 Corraling Fixture

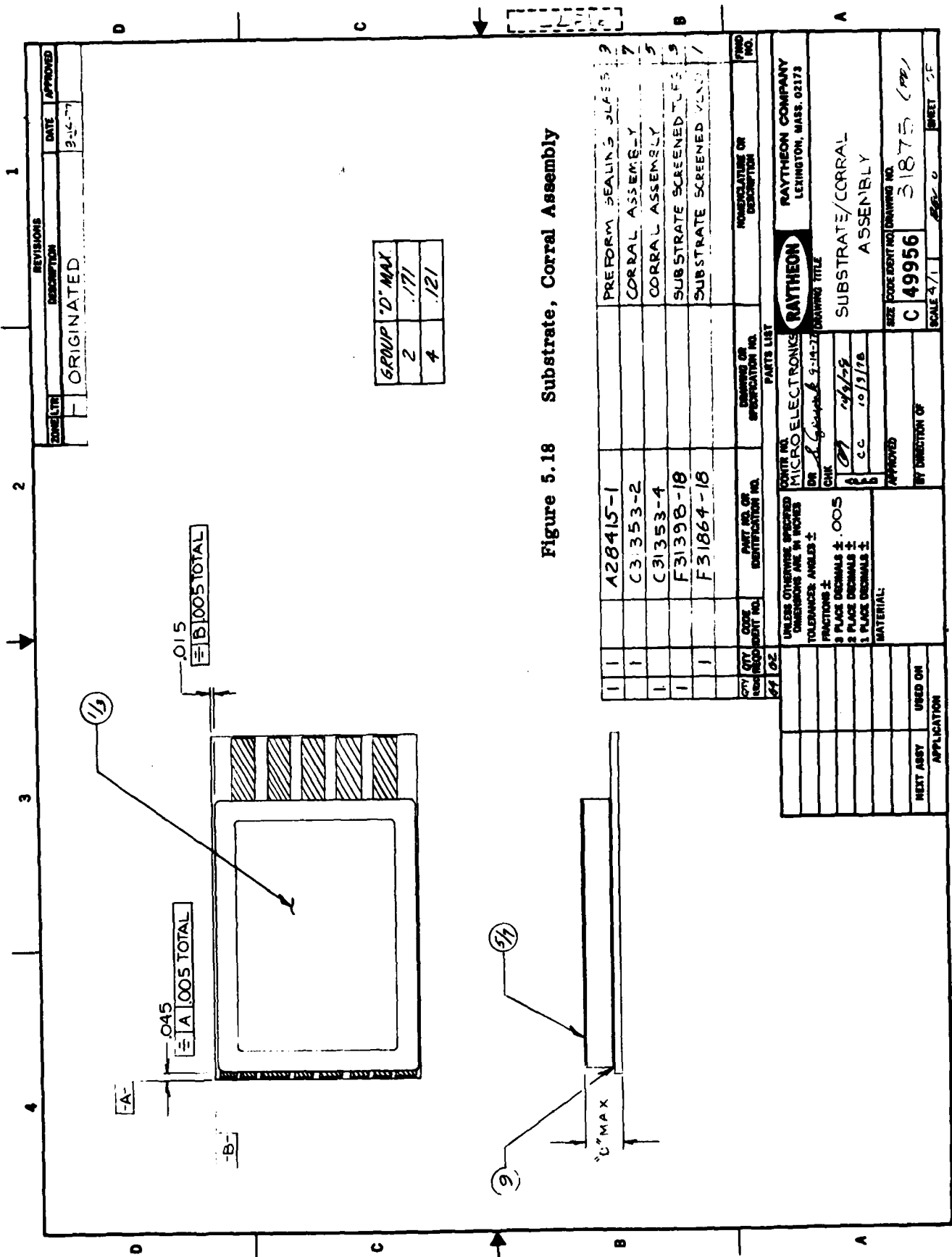


Figure 5.18 Substrate, Corral Assembly

<b>RAYTHEON</b> MICROELECTRONICS LEXINGTON, MASS. 02173	
DRAWING TITLE SUBSTRATE/CORRAL ASSEMBLY	
SIZE C 49956	CODE IDENT NO. 31875 (REV)
SCALE 1/1	
SHEET 62	

CONTROL NO. 128415-1	PART NO. OR IDENTIFICATION NO. 128415-1
QTY 1	QTY 1
CODE 1	CODE 1
DESCRIPTION PREFORM SEALING PLATES	DESCRIPTION CORRAL ASSEMBLY
PART NO. OR IDENTIFICATION NO. C3353-2	PART NO. OR IDENTIFICATION NO. C31353-4
QTY 1	QTY 1
CODE 1	CODE 1
DESCRIPTION CORRAL ASSEMBLY	DESCRIPTION SUBSTRATE SCREENED TFE
PART NO. OR IDENTIFICATION NO. F31398-18	PART NO. OR IDENTIFICATION NO. F31864-18
QTY 1	QTY 1
CODE 1	CODE 1
DESCRIPTION SUBSTRATE SCREENED VENT	DESCRIPTION SUBSTRATE SCREENED VENT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± FINISHES ± 3 PLACE DECIMALS ± .005 2 PLACE DECIMALS ± 1 PLACE DECIMALS ±
MATERIAL:
APPROVED BY: [Signature] DATE: 10/3/78
BY: [Signature] DATE: 10/3/78
NEXT ASSY USED ON APPLICATION

## 5.6 Passive Trimming

The design and layout of the TCVCXO have been optimized to allow for the application of the controllable and programmable characteristics of commercially available YAG laser trimmers to the adjustment of components to precise values. Passive trimming of the circuit substrates is carried out in the absence of active circuit elements, with no power applied to the circuit. The only electrical parameter measured is dc resistance. Operation Standards 1748 and 1754 define test and set-up requirements for TCFG and VCXO modules, respectively. The probe fixtures are illustrated in Figures 5.19 and 5.20; while the laser trimmer is shown in Figures 5.21 and 5.22.

## 5.7 Discrete Component Selection

Based on the electrical schematic included in ERADCOM technical requirements SCS-483, a parts list was generated for the chip components used in the TCVCXO module, and amended as required by subsequent changes. The final parts list appears in Table 5-1. Active chip components are selected not only with reference to functional type number but also with regard to geometry and mechanical considerations. Electrically equivalent chips from different manufacturers have to be checked to ensure compatibility with the circuit layout and with the processes employed to achieve electrical connections to the chip. As an indication of the problems encountered in this area, transistors  $Q_1$  and  $Q_3$  (2N2857) are available from two sources; one supplies high performance devices with very small bonding pads, which result in unacceptable pull test failure levels; while the other manufacturer supplies marginal electrical performance units with excellent mechanical properties. All semiconductor chips are gold back-plated to permit substrate attachment by eutectic bonding. In the selection of ceramic chip capacitors, an attempt was made to use military standard chip sizes wherever possible. Consequently, the CDR01 size (0.080 inch x 0.050 inch) was selected for all capacitors except C8. Capacitors C1 and C2 are, as required, high Q porcelain capacitors; the specified values are formed by paralleled-connecting smaller value units. Capacitor C8 is a non-standard size 0.1  $\mu$ f ceramic chip capacitor.



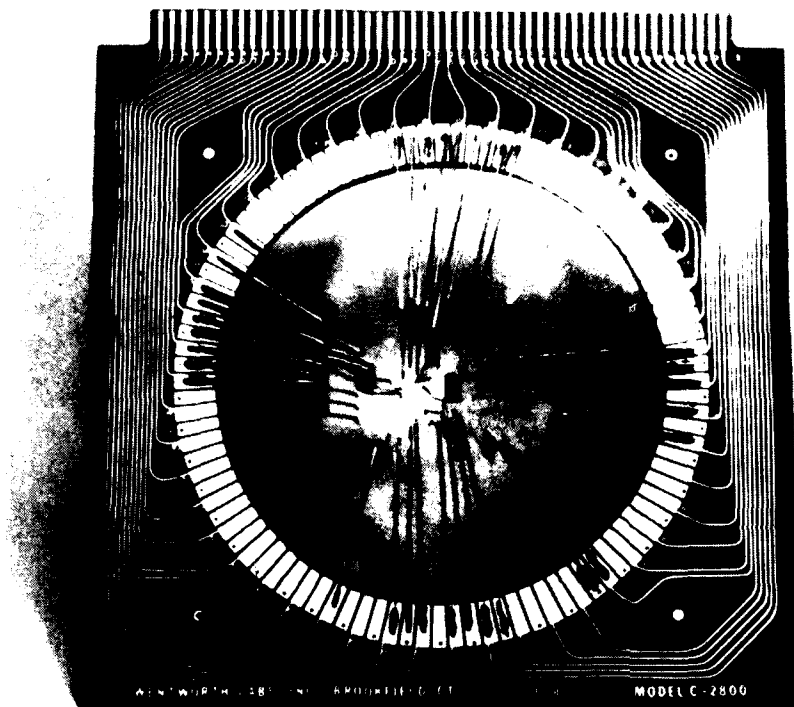


Figure 5.19  
Probe Fixture  
VCXO

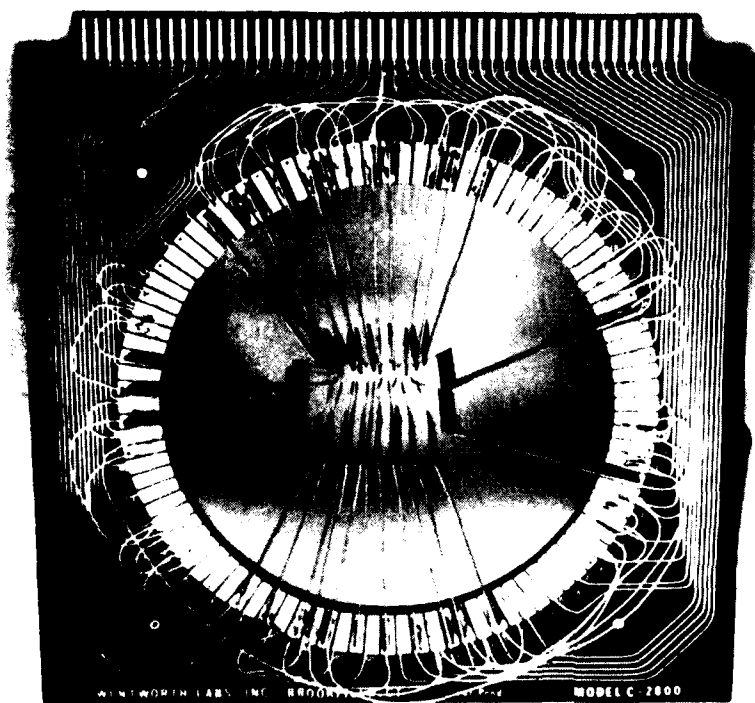
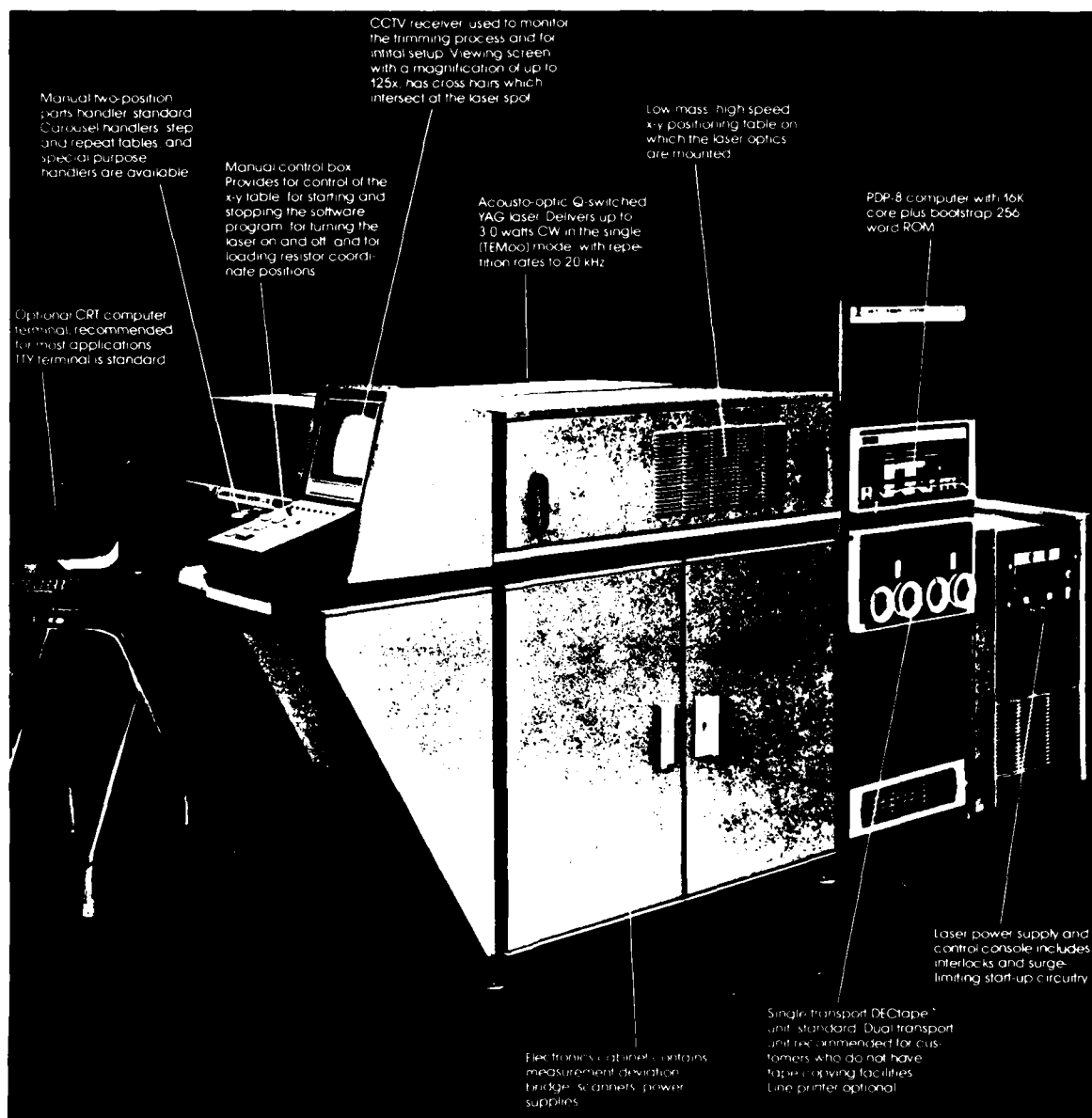


Figure 5.20  
Probe Fixture  
TCFG



**Figure 5.21 Laser Trimmer**



Figure 5.22 Laser Trimmer

TABLE 5.1 FINAL PARTS LIST (SHEET 1)

RAYTHEON		MICROWAVE AND POWER TUBE DIVISION COMPONENTS OPERATION QUINCY, MASS.		CONTROL DOCUMENT		CUSTOMER: ECON TECH-1 CUSTOMER SPEC. NO. ECS-123-AMEND. 4		PACKAGE TYPE COMST		TYPE H40380-1		REV. SH. 1 OF 2		REV. REV.	
ITEM	DESCRIPTION	QWS NO	QWS	QWS	QWS	QWS	QWS	QWS	QWS	QWS	QWS	QWS	QWS	QWS	QWS
1	EVAPORATED ANODE														
2	ONE														
3	CATHODE														
4	GRID														
5	SCREEN														
6	CONTROL														
7	MODULATOR														
8	CHINE														
9	SHIELD														
10															
11															
12	MODULAS ASSEMBLY														
13	MODULAS														
14	MODULAS														
15	MODULAS														
16	MODULAS														
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99	MODULAS														
100	MODULAS														

TABLE 5.1 FINAL PARTS LIST (SHEET 2)

RAYTHEON		MICROWAVE AND POWER TUBE DIVISION COMPONENTS OPERATION QUINCY, MASS.		CONTROL DOCUMENT		CUSTOMER: ECON - TVCX0-1 CUSTOMER SPEC. NO. 525483-AMEND. 4		PACKAGE TYPE TYPE HED300-1		REV. REV. REV. 2 OF 4		REVISIONS	
ITEM	DESCRIPTION	DWG. NO.	QTY	OPERATION STANDARDS	REMARKS								
1	SUBSTRATE - COAXIAL - CATHODE ASSEMBLY (K10)	13126-1	1										
2	WIRE	13127-1	1										
3	WIRE	13128-1	1										
4	WIRE	13129-1	1										
5	WIRE	13130-1	1										
6	WIRE	13131-1	1										
7	WIRE	13132-1	1										
8	WIRE	13133-1	1										
9	WIRE	13134-1	1										
10	WIRE	13135-1	1										
11	WIRE	13136-1	1										
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234	WIRE	13359-1	1										
235	WIRE	13360-1	1										
236	WIRE	13361-1	1										

TABLE 5.1 FINAL PARTS LIST (SHEET 3)

FORM NO. CD 1117 68

**RAYTHEON**

MICROWAVE AND POWER TUBE DIVISION  
COMPONENTS OPERATION  
QUINCY, MASS.

CONTROL DOCUMENT

CUSTOMER: ECOM TRK-10-1  
CUSTOMER BRG. NO. 53403, AMENR 4  
REV. 1  
PACKAGE TYPE CONST.

ITEM	DESCRIPTION	DWG NO	QUAN	REV	OPERATION STANDARDS	REMARKS
101	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
102	WIRE	13124-1	1			
103	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-1	1			
104	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
105	WIRE	13124-1	1			
106	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
107	WIRE	13124-1	1			
108	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
109	WIRE	13124-1	1			
110	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
111	WIRE	13124-1	1			
112	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
113	WIRE	13124-1	1			
114	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
115	WIRE	13124-1	1			
116	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
117	WIRE	13124-1	1			
118	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
119	WIRE	13124-1	1			
120	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
121	WIRE	13124-1	1			
122	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
123	WIRE	13124-1	1			
124	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
125	WIRE	13124-1	1			
126	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
127	WIRE	13124-1	1			
128	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
129	WIRE	13124-1	1			
130	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
131	WIRE	13124-1	1			
132	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
133	WIRE	13124-1	1			
134	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
135	WIRE	13124-1	1			
136	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
137	WIRE	13124-1	1			
138	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
139	WIRE	13124-1	1			
140	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
141	WIRE	13124-1	1			
142	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
143	WIRE	13124-1	1			
144	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
145	WIRE	13124-1	1			
146	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
147	WIRE	13124-1	1			
148	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
149	WIRE	13124-1	1			
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151	WIRE	13124-1	1			
152	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
153	WIRE	13124-1	1			
154	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
155	WIRE	13124-1	1			
156	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
157	WIRE	13124-1	1			
158	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
159	WIRE	13124-1	1			
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161	WIRE	13124-1	1			
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163	WIRE	13124-1	1			
164	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
165	WIRE	13124-1	1			
166	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
167	WIRE	13124-1	1			
168	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
169	WIRE	13124-1	1			
170	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
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177	WIRE	13124-1	1			
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184	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
185	WIRE	13124-1	1			
186	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
187	WIRE	13124-1	1			
188	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
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190	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
191	WIRE	13124-1	1			
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194	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
195	WIRE	13124-1	1			
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197	WIRE	13124-1	1			
198	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			
199	WIRE	13124-1	1			
200	SUBSTRATE - 1/2" x 1/2" x 1/2" (TYP)	13124-2	1			

TABLE 5.1 FINAL PARTS LIST (SHEET 4)

FORM NO. CD 1117-40

RAYTHEON

MICROWAVE AND POWER TUBE DIVISION  
COMPONENTS OPERATION  
QUINCY, MASS.

CONTROL DOCUMENT

CUSTOMER: ECOM TENANT-1  
CUSTOMER P.O. NO. EC5483 APPEND. 4  
REV. 1

PACKAGE TYPE  
CONST  
TYPE  
MOSBY-1  
REV. 1  
REVISIONS

ITEM	DESCRIPTION	DWG. NO.	QUAN.	PDC	OPERATION STANDARDS	REMARKS
1	SCHEMATIC (TEAM)	2334	3	3		
2	SCHEMATIC (TEAM)	2334	3	3		
3	SCHEMATIC (TEAM)	2334	3	3		
4	SCHEMATIC (TEAM)	2334	3	3		
5	SCHEMATIC (TEAM)	2334	3	3		
6	SCHEMATIC (TEAM)	2334	3	3		
7	SCHEMATIC (TEAM)	2334	3	3		
8	SCHEMATIC (TEAM)	2334	3	3		
9	SCHEMATIC (TEAM)	2334	3	3		
10	SCHEMATIC (TEAM)	2334	3	3		
11	SCHEMATIC (TEAM)	2334	3	3		
12	SCHEMATIC (TEAM)	2334	3	3		
13	SCHEMATIC (TEAM)	2334	3	3		
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17	SCHEMATIC (TEAM)	2334	3	3		
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28	SCHEMATIC (TEAM)	2334	3	3		
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44	SCHEMATIC (TEAM)	2334	3	3		
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54	SCHEMATIC (TEAM)	2334	3	3		
55	SCHEMATIC (TEAM)	2334	3	3		
56	SCHEMATIC (TEAM)	2334	3	3		
57	SCHEMATIC (TEAM)	2334	3	3		
58	SCHEMATIC (TEAM)	2334	3	3		
59	SCHEMATIC (TEAM)	2334	3	3		
60	SCHEMATIC (TEAM)	2334	3	3		
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63	SCHEMATIC (TEAM)	2334	3	3		
64	SCHEMATIC (TEAM)	2334	3	3		
65	SCHEMATIC (TEAM)	2334	3	3		
66	SCHEMATIC (TEAM)	2334	3	3		
67	SCHEMATIC (TEAM)	2334	3	3		
68	SCHEMATIC (TEAM)	2334	3	3		
69	SCHEMATIC (TEAM)	2334	3	3		
70	SCHEMATIC (TEAM)	2334	3	3		

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FROM COPY FURNISHED TO DDC

A military standard 0.1  $\mu$ f capacitor is available in a CDR04 configuration (0.180 inch x 0.125 inch), but this was determined to be too large for use in the crowded VCXO submodule. Capacitor terminations are palladium-silver to ensure compatibility with the solder employed for mechanical attachment and electrical connection.

Detail specifications for semiconductor chips appear in Figures 5.23 - 5.30; for capacitors, Figures 5.31 and 5.32.

### 5.8 Component Attachment

Silicon semiconductor chips are bonded to the substrate through the formation of a gold-silicon eutectic. This is accomplished through the use of the equipment illustrated in Figure 5.33. The bonder is fitted with a specific collet for each chip dimension; the mirror serves to orient the chip properly before it is picked up in the collet. The substrate is pre-warmed on a hot plate set to a specified temperature. It is then placed in the heat column, where it is held down by a vacuum. The semiconductor chip in the die collet is then moved into proper position over the bonding site on the substrate; the bond is formed through the rubbing action imparted by vibrating the collet, and through the heat generated in the column. The bond is inspected visually, and the unit is removed and stored upside down to prevent damage to the circuit. (Ref. O.S. 1025).

Electrical connections between the substrate and the semiconductor chips are established through the attachment of very fine gold wires between the required interfaces by ultrasonic bonding techniques (Ref. O.S. 1029). Figure 5.34 illustrates the ultrasonic wire bonder. Capacitor chips are mounted on the substrate by reflow soldering, using a silver-bearing tin-lead alloy solder (Ref. O.S. 1494). After cleaning and inspection, the units are stored upside down in sealed nitrogen-filled cabinets to await further processing.




APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED

H60388

NOTES :

A-- MUST MEET ALL APPLICABLE REQUIREMENTS OF  
RAYTHEON DWG. 28098.

Figure 5.23

REV STATUS OF SHEETS	REV LTR																			SPECIFICATION CONTROL DRAWING
	SHEET NO.																			
<small>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES</small> <small>ANGLES ±</small> <small>DECIMALS ±</small> <small>FRACTIONS ±</small> <small>INCHES ±</small>		CONTR NO.		<div style="border: 1px solid black; border-radius: 50%; padding: 5px; display: inline-block;"> <b>RAYTHEON</b> </div>		<b>RAYTHEON COMPANY</b> LEXINGTON, MASS. 02173														
		DR	EC5			9-13-77	DRAWING TITLE													
		CHK			DIODE IN751A															
		A P P R O V E D																		
APPROVED				SIZE	CODE IDENT NO.	DRAWING NO.														
BY DIRECTION OF		RMC-6677		A	49956	32145														
				SCALE	1/4"	REV.	SHEET													

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APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED

*H60388*

NOTES :

*A - MUST MEET ALL APPLICABLE REQUIREMENTS OF  
RAYTHEON DWG. 28098.*

Figure 5.25

REV STATUS OF SHEETS	REV LTR																	SPECIFICATION CONTROL DRAWING
	SHEET NO.																	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		CONTR NO.		RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS. 02173												
TOLERANCES: ANGLES $\pm$		DR <i>263</i>																<i>1-13-77</i>
FRACTIONS $\pm$		CHK		DRAWING TITLE														
3 PLACE DECIMALS $\pm$		A		<i>DIODE</i> <i>IN3600</i>														
2 PLACE DECIMALS $\pm$		P																
1 PLACE DECIMALS $\pm$		D																
MATERIAL:		APPROVED <i>R. H. Zick</i>		SIZE	CODE IDENT NO.	DRAWING NO.												
		BY DIRECTION OF <i>POC 79-6697</i>		<i>A</i>	<i>49956</i>	<i>32142</i>												
				SCALE <i>1/4"</i>	<i>REV. 1</i>	SHEET												

10-2736 (6-72) VELLUM PRINTED IN U.S.A.

APPLICATION			REVISIONS											
NEXT ASSY	USED ON	LTR	DESCRIPTION							DATE	APPROVED			
<i>H60388</i>														
<p><i>NOTES:</i></p> <p><i>A - MUST MEET ALL APPLICABLE REQUIREMENTS OF</i> <i>RAYTHEON DWG. 28098</i></p>														
REV STATUS OF SHEETS		REV LTR											SPECIFICATION CONTROL DRAWING	
		SHEET NO.												
<small>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES</small>  TOLERANCES: ANGLES $\pm$ FRACTIONS $\pm$ 3 PLACE DECIMALS $\pm$ 2 PLACE DECIMALS $\pm$ 1 PLACE DECIMALS $\pm$ MATERIAL:			CONTR NO.		<div style="border: 1px solid black; border-radius: 50%; padding: 5px; display: inline-block;"><b>RAYTHEON</b></div>		<b>RAYTHEON COMPANY</b> <small>LEXINGTON, MASS. 02173</small>							
			DR <i>EC3</i>								<i>943-7</i>			
			CHK		DRAWING TITLE  <div style="font-size: 1.2em; font-family: cursive;">DIODE IN 4567</div>									
			APPD											
			APPROVED		SIZE	CODE IDENT NO.	DRAWING NO.							
			BY DIRECTION OF		A	49956	32149							
<i>RMW</i>			<i>PO179-6697</i>		SCALE <i>1X</i>		REV <i>1</i>		SHEET					

Figure 5.26





APPLICATION			REVISIONS			
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H60388

NOTES:

A - MUST MEET ALL APPLICABLE REQUIREMENTS OF  
RAYTHEON DWG. 28098

Figure 5.29

REV STATUS OF SHEETS	REV LTR																	SPECIFICATION CONTROL DRAWING
	SHEET NO.																	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		CONTR NO.		RAYTHEON		RAYTHEON COMPANY LEXINGTON, MASS. 02173												
TOLERANCES: ANGLES $\pm$		DR <i>EEJ</i>		9-13-71		DRAWING TITLE <i>TRANSISTOR</i> <i>ZN2907A</i>												
FRACTIONS $\pm$		CHK																
3 PLACE DECIMALS $\pm$		A																
2 PLACE DECIMALS $\pm$		P																
1 PLACE DECIMALS $\pm$		D																
MATERIAL:		APPROVED		SIZE		CODE IDENT NO.		DRAWING NO.										
		<i>R. M. Tell</i>		A		49956		<i>32147</i>										
		BY DIRECTION OF		SCALE		REV. 1		SHEET										
		<i>POC 79-6697</i>		<i>H</i>														

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APPLICATION				REVISIONS												
NEXT ASSY	USED ON	LTR	DESCRIPTION								DATE	APPROVED				
<div style="text-align: center; margin-bottom: 20px;"><i>H60388</i></div> <div style="text-align: center; margin-top: 300px;"> <p>Figure 5.32</p> <p><i>100 pf ± 5% 100V</i></p> </div>																
REV STATUS OF SHEETS	REV LTR															SPECIFICATION CONTROL DRAWING
	SHEET NO.															
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES  TOLERANCES: ANGLES ± FRACTIONS ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ± 1 PLACE DECIMALS ± MATERIAL:		CONTR NO.		<div style="border: 2px solid black; border-radius: 15px; padding: 5px; display: inline-block;">RAYTHEON</div>		RAYTHEON COMPANY LEXINGTON, MASS. 02173										
		DR														
		CHK		DRAWING TITLE <div style="font-size: 1.2em; margin-top: 10px;"><i>CAPACITOR</i></div> <div style="font-size: 1.2em; margin-top: 5px;"><i>W100BC101J5</i></div>												
		A														
		P														
D		APPROVED		SIZE	CODE IDENT NO.	DRAWING NO.										
BY DIRECTION OF				A	49956	32151										
				SCALE . <i>H</i>		REV. 0				SHEET						

10-2736 (6-72) VELLUM PRINTED IN U.S.A.

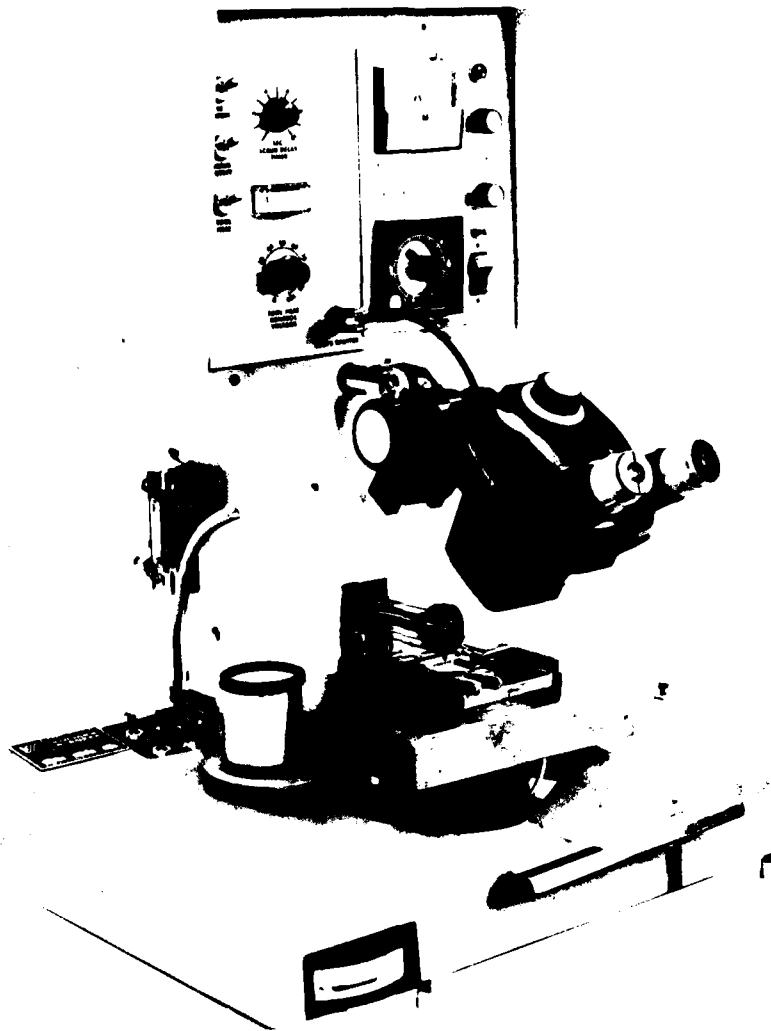


Figure 5.33 Die Bonding Equipment

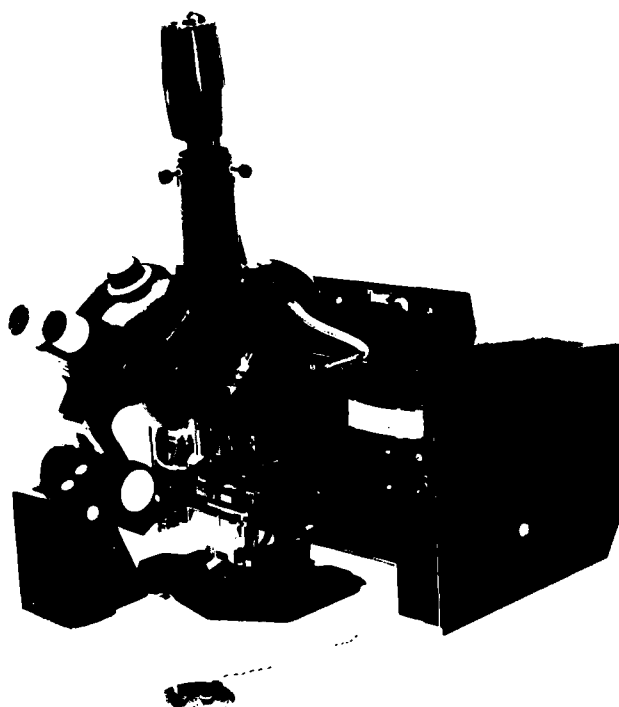


Figure 5.34 Ultrasonic Wire Bonder

### 5.9 Active Laser Trimming

Following the attachment of chip components to the substrate and the completion of all electrical interconnections within the submodules, active trimming of the units is undertaken in accordance with O.S. 1652 for the TCFG module, and O.S. 1653 for the VCXO module. Both procedures are derived from the ERADCOM supplied active trim procedure (Appendix C).

Special probe cards and test fixtures have been designed to facilitate interfacing with both the laser trimmer and the test equipment required to perform electrical tests (Figure 5.35).

Temporary connections are established between the VCXO submodule and its assigned quartz crystal during active trim; crystal and submodule identification numbers are recorded to guarantee proper remating of corresponding parts at final module assembly.

### 5.10 Submodule Sealing

After active laser trim, the submodules are ready for sealing per O.S. 1753. The lids for the TCFG module, and the VCXO modules intended to mate with ceramic or HC-18 crystals are identical (Figure 5.36). The lid for VCXO modules using the TO-5 packaged crystals (Figure 5.37) is provided with a recess (Figure 5.37) for the crystal such that the total assembly can fit within the diallyl phthalate case.

The sealing process is carried out in vacuo within an automatic machine which seals the four sides of the rectangular lid in one operation. The corralled substrate is nested within the seam-sealer fixture, and a gold-tin preform and then the lid are positioned over the corral. The unit then passes under a set of opposing rolling electrodes which apply both controlled pressure and pulsed current; this seals two parallel sides; the unit is then rotated 90° and the process is repeated, thereby sealing the other two sides of the lid to the corral. Figure 5-38 illustrates the seam sealer, and Figure 5.39, the electrodes and the seam-sealer nest.



Figure 5.35A Laser Trimmer Substrate Interface (TCFG)

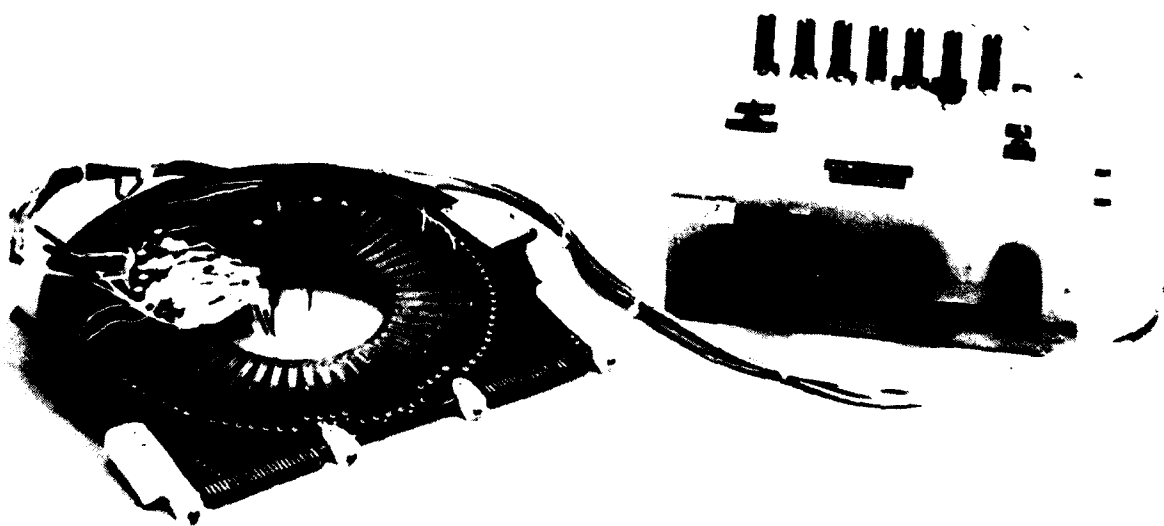


Figure 5.35B Laser Trimmer Substrate Interface (CVXO)

AD-A086 022

RAYTHEON CO QUINCY MASS INDUSTRIAL COMPONENTS OPERATION F/6 9/5  
MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM&TE) PROGRA--ETC(U)  
APR 80 R M ZILBERSTEIN DAAB07-76-C-8119

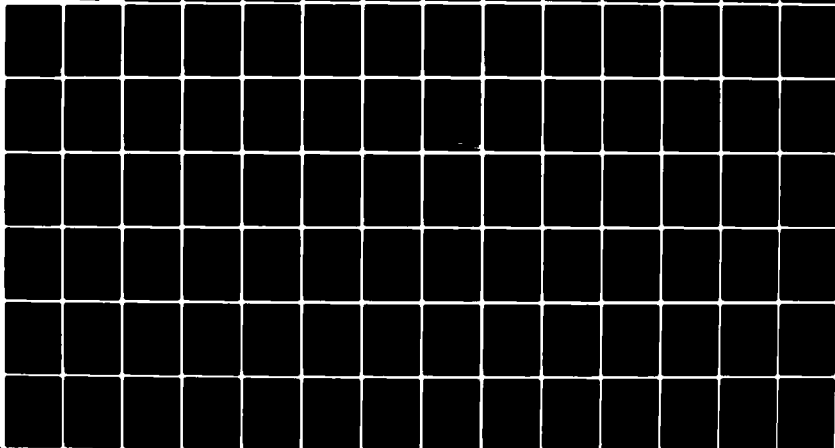
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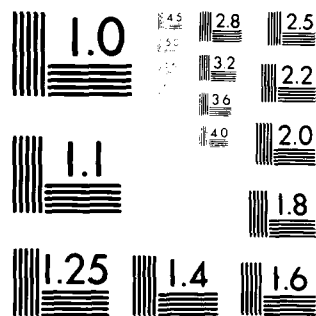
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MICROCOPY RESOLUTION TEST CHART  
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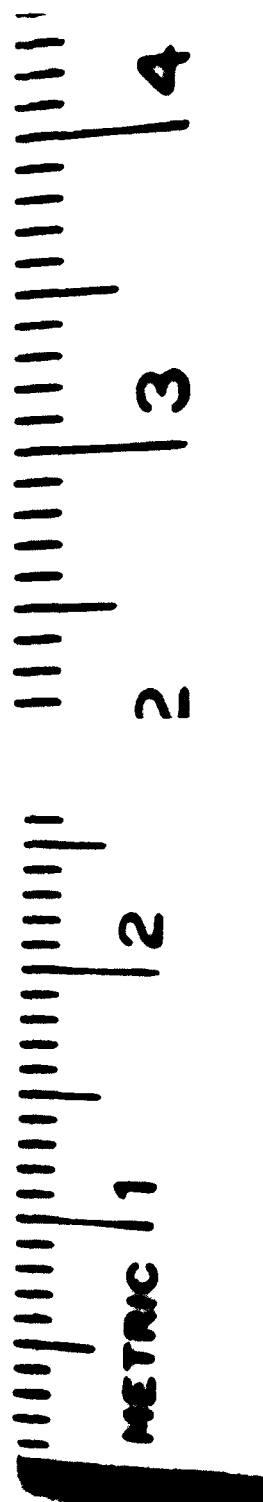
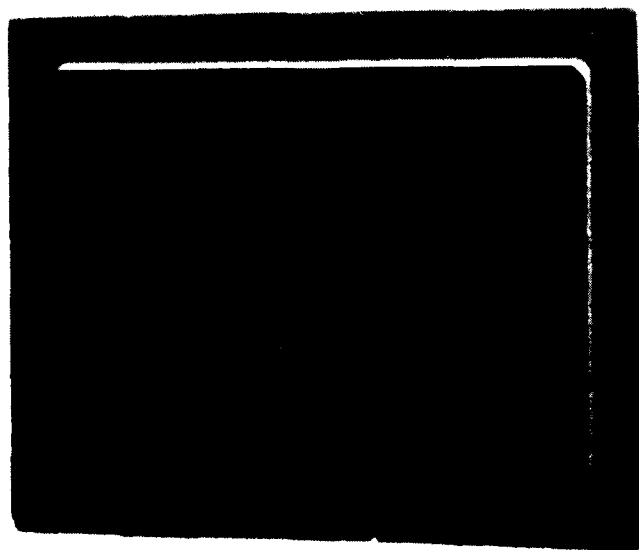


Figure 5.36 Corral Lid and Crystal Spacer - HC18 and Ceramic Crystal

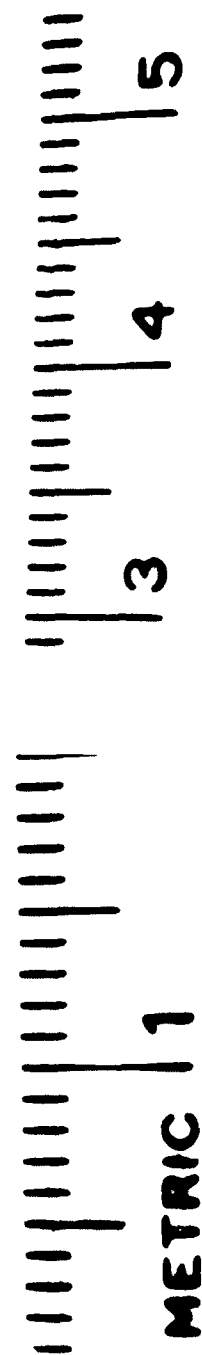
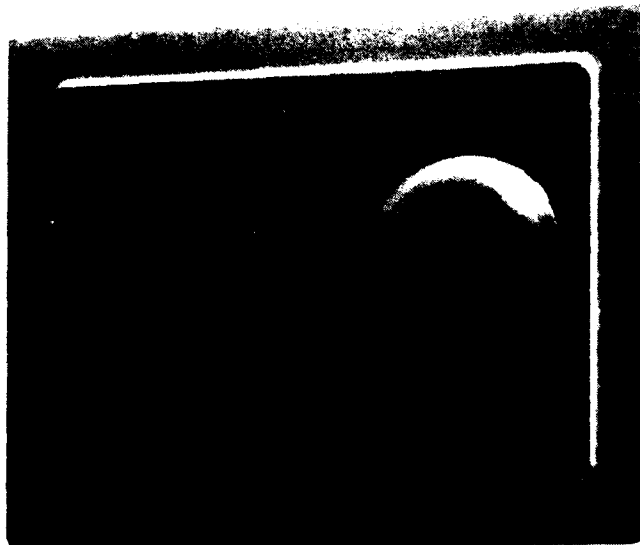
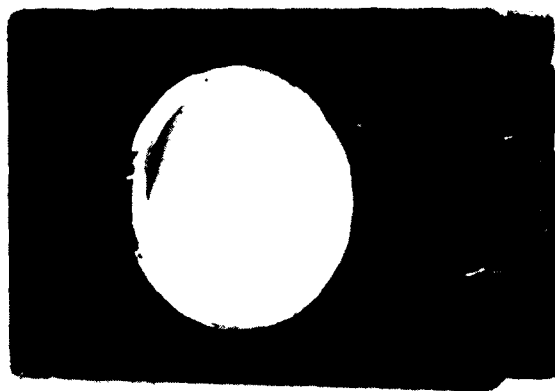


Figure 5.37 Corral Lid and Crystal Spacer - T05 Crystal

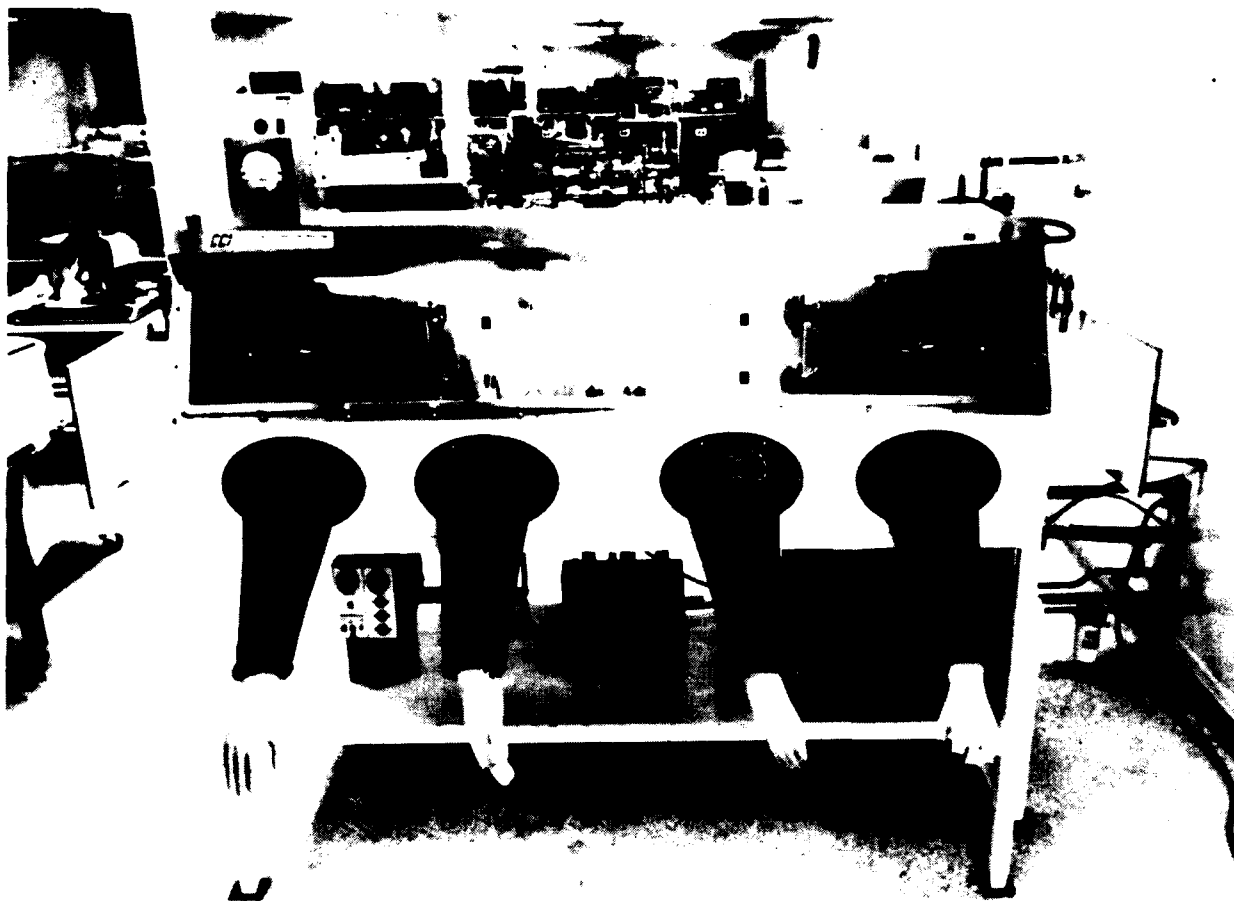
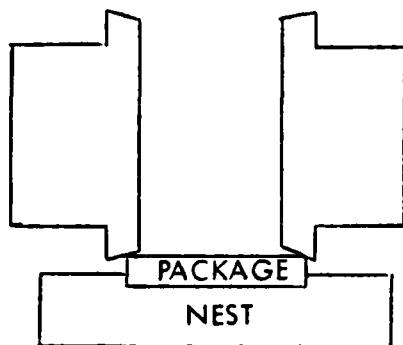


Figure 5.38 Seam Sealer



ELECTRODE No. 102-217B

Matl: RWMA-3 Alloy  
(Mallory #100)

Figure 5.39 Electrodes and Seam-Seal Nest

No. 102-202  
Matl: Copper

### 5.11 VCXO Crystal Potentiometer Assembly

After sealing, the VCXO submodule is permanently mated with its assigned crystal. Three crystal mounting techniques have been evolved, one for each of the three package types. The crystal is first epoxy-glued to an aluminum spacer which is, in turn, epoxied to the specified area of the lid. The TO-5 crystal, in its perforated spacer, is fitted over the dimple of the lid. Electrical connections are completed by splicing solid wire extensions to the crystal leads (applying insulating teflon tubing over the leads if necessary) and soldering to the specified tabs on the module. The potentiometer assembly is similarly mounted on the lid and connected to the specified tabs. O.S. 1758 details these procedures.

### 5.12 Mating of Submodules

Mating of the sealed submodules is accomplished by epoxy cementing a TCFG module and a VCXO module back-to-back, after interconnecting copper ribbon loops have been soldered to the pads located at the rear of each substrate (Ref. O.S. 1759).

### 5.13 Module Encapsulation and Marking

The completed module is inserted into the diallyl phthalate case, and an epoxy resin is poured into the case after masking off those areas which are to remain resin-free (O.S. 1763). Following a cure at 80°C for one hour, the units are solvent-cleaned and marked with epoxy ink per O.S. 1766.

### 5.14 Packaging and Shipment

Units are shipped in foam-rubber partitioned cardboard containers per O.S. 1767.

## 6.0 MODULE TESTING

### 6.1 General

Definitions, test procedures, and test set-ups conform to the guidelines set forth in MIL-0-55310, and to the requirements of ERADCOM Technical Requirement SCS 483.

### 6.2 Test Data Forms

Final data for each module are presented on the test data form shown in Figure 6.1. Additionally, frequency versus temperature data for three modulation voltage levels, presented in graphical form, are attached to the final test data form; a typical set of such curves is shown in Figure 6.2. Prepot test measurements (which are kept for reference only and are not supplied to the customer) are recorded on the test data form illustrated in Figure 6.3. The performance limits specified therein are offset to allow for the effects of epoxy encapsulation on the final performance of the device. Measurements performed at various other stages of manufacture in accordance with specific Raytheon Operation Standard, are not normally recorded on formal test data sheets.

### 6.3 Test Fixtures

A Functional Test Box (Figure 6.4) was designed to permit module testing, not only at the final stage but also at various stages of fabrication. It provides the proper interfacing with the functional test probes employed for active trimming of both VCXO and TCFG modules, and permits all required tests to be performed on the submodules. The schematic is pictured in Figure 6.5.

To comply with the requirement that frequency measurements be made continuously over the temperature range at both nominal centre frequency and at minimum and maximum modulation level, an electronic switch was constructed to apply the proper



# TEST DATA

TCVCX0 - P/N H60388, rev. \_\_\_\_  
SCS-483 Amend. 5 Preliminary

S/N \_\_\_\_\_ Xtal Lot Letter \_\_\_\_\_ Dash Number \_\_\_\_\_

Tested by \_\_\_\_\_ Date \_\_\_\_\_

Appd. by \_\_\_\_\_ Date \_\_\_\_\_

TCVCX0 Lot No. \_\_\_\_\_

TEST NO.	PARAMETER	LIMITS		UNIT	READING	ACC(A) REJ.(R)
		MIN.	MAX.			
1.	Freq. Adj. Range	21,937,390	21,937,609	Hz	Check: HF O.K. ____ LF O.K. ____	____
2.	Freq. Dev.	21,937,---	21,937,---		Freq. (3 digits) TPI (volt)	
	FC	_ 498	_ 502	Hz	____	____
	+ Analog	_ 085	_ 165	Hz	____	____
	+ FSK - Space	_ 154	_ 221	Hz	____	____
	- FSK - Mark	_ 779	_ 846	Hz	____	____
	- Analog	_ 835	_ 915	Hz	____	____
3.	Input Impedance	180	220	K $\Omega$	____	____
4.	Input Power at +16 V	—	4	ma	____	____
5.	DC Output					
	16V - no load	8.980	9.020	V	____	____
	10V - 1 ma load	8.980	9.020	V	____	____
	-40°C	8.980	9.020	V	____	____
	+75°C	8.980	9.020	V	____	____
6.	Freq. - Volt. Stab. (10-16V)	—	5.5	Hz	____	____
7.	Freq. - Load Stab. (1.2K-0.8K $\Omega$ )	—	5.5	Hz	____	____
8.	RF Output	1.0	—	V	____	____
9.	Modulation B.W.					
	Sine Wave - 8K Hz	—	3	db	____	____
	Square Wave - 1.2K Hz	—	3	db	____	____

## 10. $\Delta F$ Temp. Curve Data:

F max. \_\_\_\_ F min. \_\_\_\_ F<sub>30</sub> \_\_\_\_ F<sub>25</sub> \_\_\_\_

$$\Delta F = F_{30} - \frac{1}{2} (F \text{ max.} + F \text{ min.}) = \underline{\hspace{2cm}}$$

## 11. Set Freq. to $\Delta F + (F_{25} - F_{30})$ \_\_\_\_\_

## 12. Freq. deviation at $\Delta F$ setting (reference only)

21,93\_\_\_\_ (enter last 4 digits)

F<sub>C</sub> \_\_\_\_\_  
+ Analog \_\_\_\_\_  
+ FSK - Space \_\_\_\_\_  
- FSK - Mark \_\_\_\_\_  
- Analog \_\_\_\_\_

Figure 6.1 Final Test Data Form

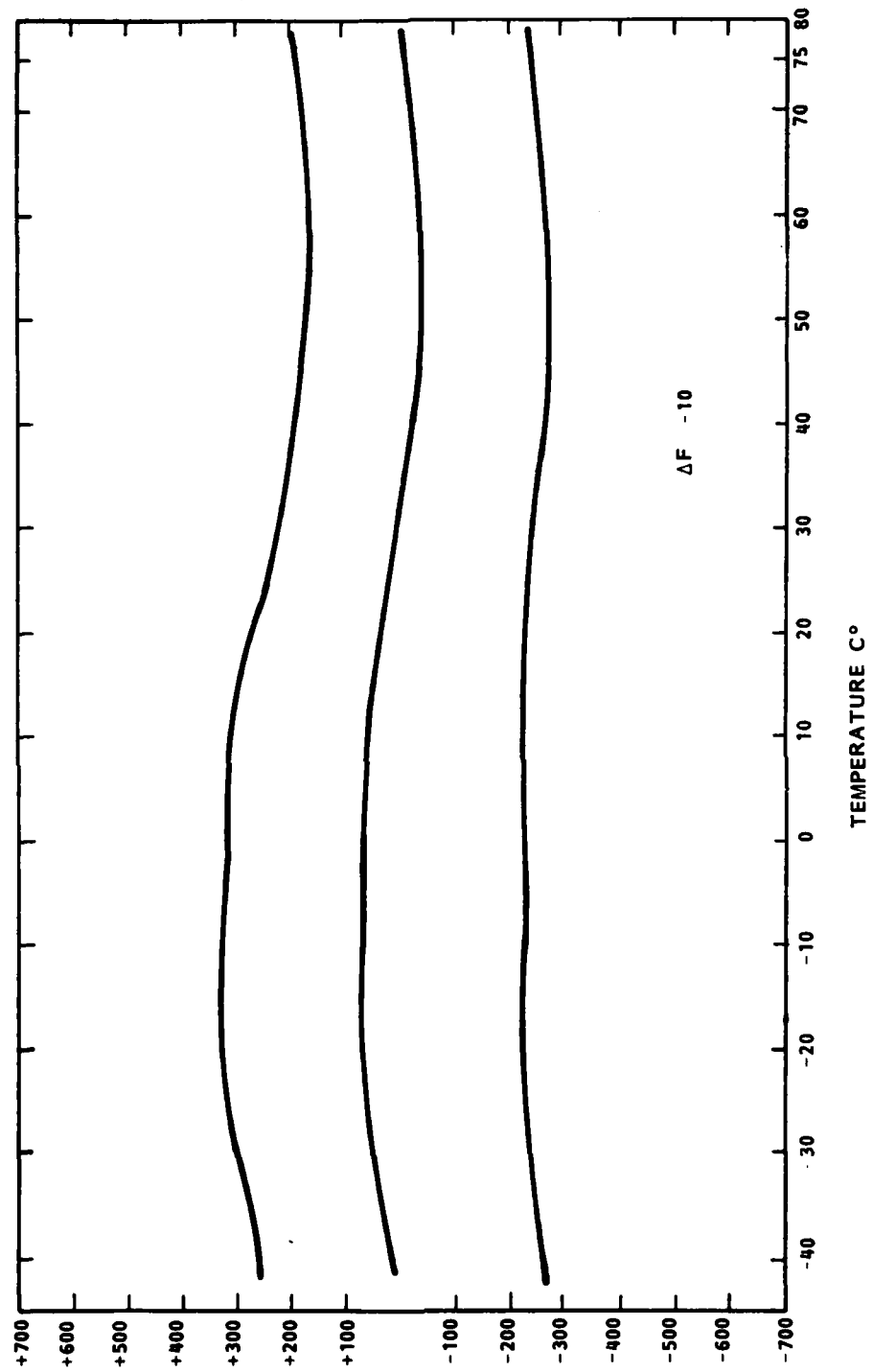


Figure 6.2 Typical Frequency vs Temperature Curve



# PRE-POT TEST DATA

TCVCXO - P/N H60388, rev. \_\_\_\_  
SCS-483 Amend.5 Preliminary

S/N \_\_\_\_\_ Xtal Lot Letter \_\_\_\_\_ Dash Number \_\_\_\_\_

Tested by \_\_\_\_\_ Date \_\_\_\_\_

Appd. by \_\_\_\_\_ Date \_\_\_\_\_

TCVCXO Lot No. \_\_\_\_\_

TEST NO.	PARAMETER	LIMITS		UNIT	READING	ACC(A) REJ(R)
		MIN.	MAX.			
1.	Freq. Adj. Range	21,937,390	21,937,620	Hz	Check: HF O.K. ____ LF O.K. ____	____
2.	Freq. Dev.	21,937, ___	21,937, ___		Freq. (3 digits) TPI (volt)	
	FC	___ 498	___ 502	Hz	____	____
	+Analog	___ 80	___ 150	Hz	____	____
	+FSK-Space	___ 150	___ 210	Hz	____	____
	-FSK-Mark	___ 790	___ 850	Hz	____	____
	-Analog	___ 850	___ 920	Hz	____	____
3.	Input Impedance	180	220	K.Ω	_____	____
4.	Input Power at +16V	—	4	ma	_____	____
5.	DC Output					
	16V - no load	8.980	9.020	V	_____	____
	10 V - 1 ma load	8.980	9.020	V	_____	____
	-40°C	8.980	9.020	V	_____	____
	+75°C	8.980	9.020	V	_____	____
6.	Freq. - Volt. Stab. (10-16V)	—	5.5	Hz	_____	____
7.	Freq. - Load Stab. (1.2K - 0.8K Ω)	—	5.5	Hz	_____	____
8.	RF Output	1.0	—	V	_____	____
9.	Modulation B.W.					
	Sine Wave - 8K Hz	—	3	db	_____	____
	Square Wave - 1.2K Hz	—	3	db	_____	____
10.	Temp. Curve	—	—	—	O.K. ____	____

Figure 6.3 Prepot Test Data Form



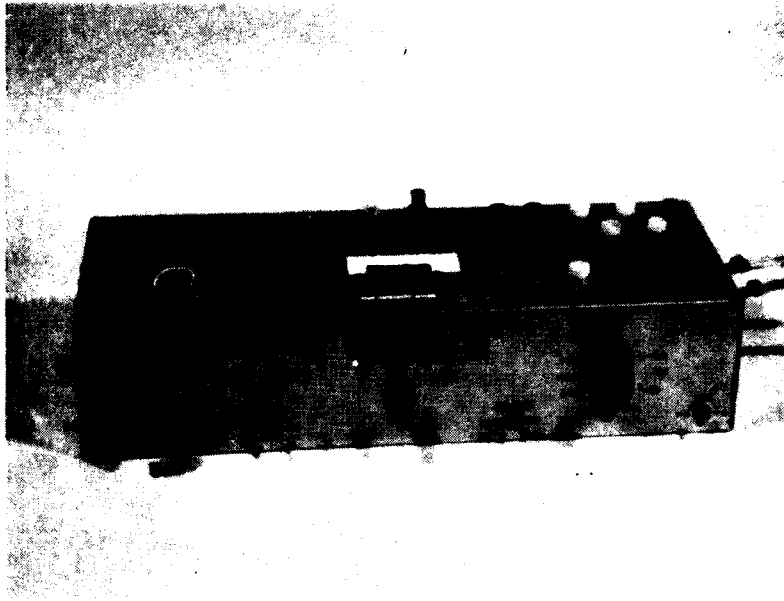


Figure 6.4    Functional Test Box

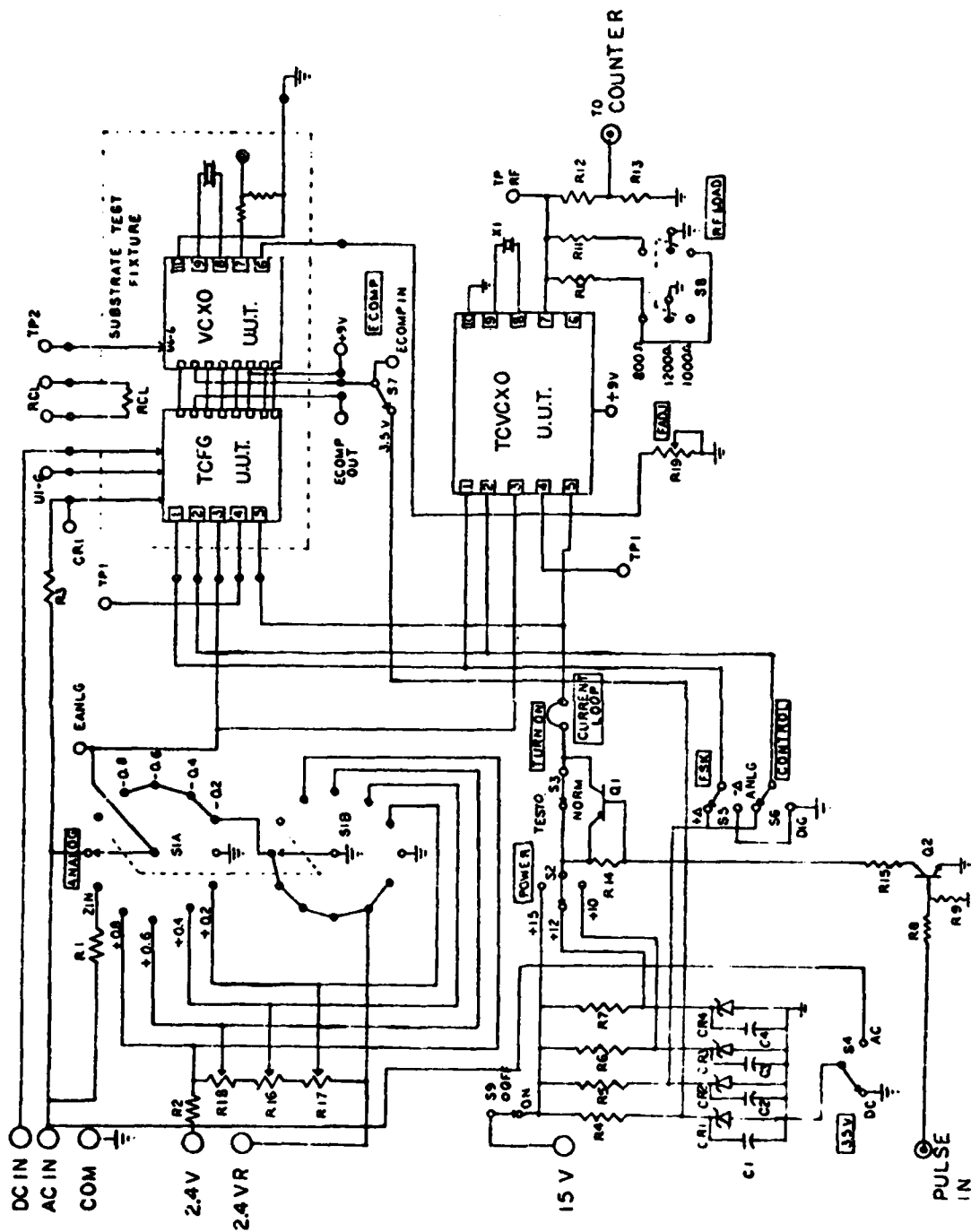


Figure 6.5 Test Box Schematic

modulation voltages sequentially at each temperature. The schematic appears in Figure 6.6.<sup>1</sup>

#### 6.4 Test Plan

The formal test plan for the TCVCXO module is presented in Appendix D.

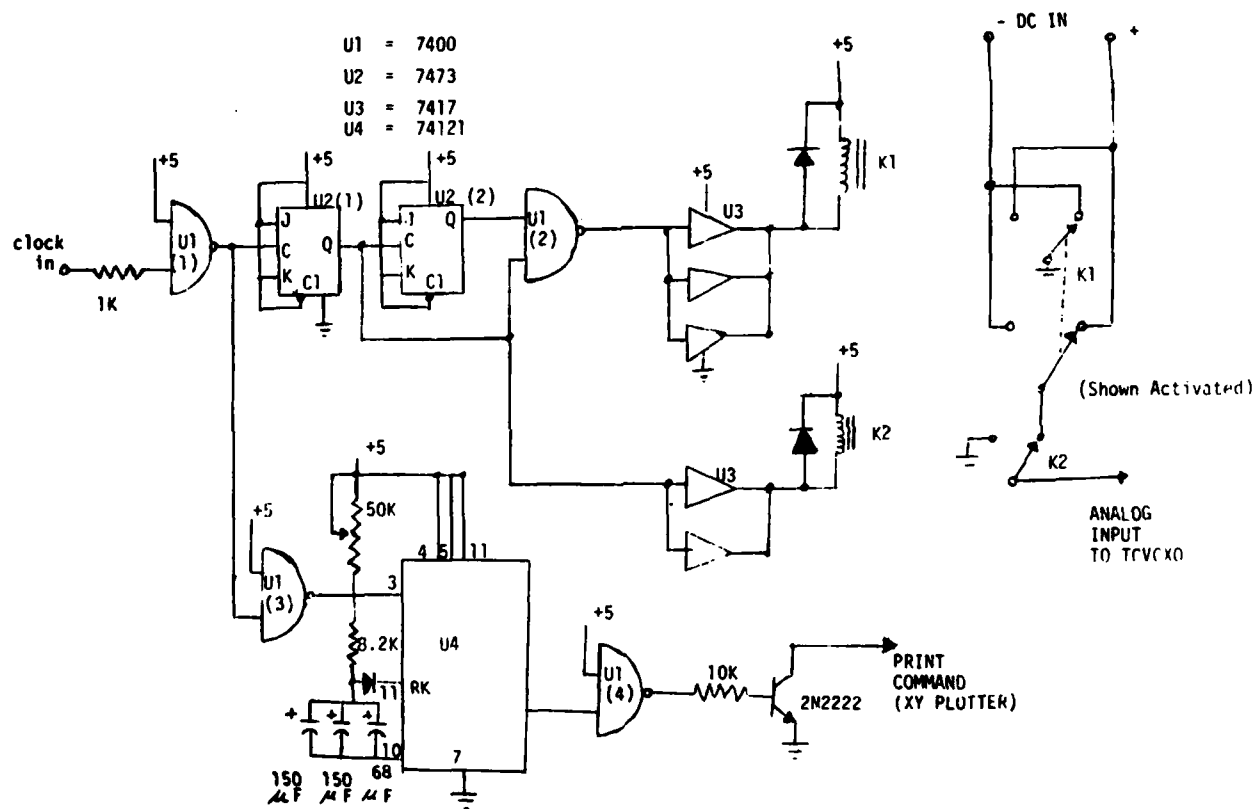


Figure 6.6 Electronic Switch Schematic

1. Circuit operation was described in the Third Quarterly Progress Report, pages 12 and 17.

## 7.0 CONCLUSIONS

The utilization of thick-film hybrid techniques in the design and construction of wide-range, high-reliability TCVCXO's has been successfully demonstrated. The technology developed for this application is fully compatible with high performance rf circuitry; clearly, it does not dilute the reliability of the quartz crystal resonator, whose performance is central to the operation of the TCVCXO. The electrical requirements set forth in ERADCOM document SCS 483 have been met by the majority of units; while all devices incorporating crystals capable of meeting the mechanical requirements have met those requirements fully.

The corral technique adopted for the final TCVCXO design appears to provide substantial advantages in terms of achievable component densities. Despite the difficulties involved in pretesting active devices in chip form, repairs are relatively easy to perform before the corral is sealed, and are even possible after sealing. The major undisputed advantage over competing approaches, such as chip carriers, is the access of all interconnections to visual inspection. The only obvious improvement over the present technique would be to segregate active and passive components, with only the former enclosed within the corral. The wide range in resistor values presented by the mix of rf and analog circuits did not prove to be a major stumbling block, despite the large number of screenings and firings involved. The project also demonstrated that active laser trim of rf circuits is possible provided proper fixturing and interfacing procedures are established.

While yields and production costs did not fall within the projected limits, for reasons already discussed, large scale production, rather than piecework, and the availability of the quartz crystals specifically designed for this application, should do much to rectify the situation.

## 8.0 RECOMMENDATIONS FOR FUTURE WORK

### 8.1 Introduction

The present design and manufacturing techniques used in the fabrication of the TCVCXO circuits permit the production of units in small and medium scale quantities. However, the need to produce devices in greater volume, with an accompanying reduction in the cost of individual modules, demands changes in the physical and electrical design, component selection, production procedures, and test methods.

The problem has to be addressed at several levels, including reduction of component and material cost, decrease in manufacturing labor, increase in manufacturing yield, and improvement of critical performance characteristics such as frequency deviation and temperature frequency stability.

At present, the TCVCXO is made by fabricating separate VCXO and TCFG modules (see Figure 4.8 for circuit partitioning), marrying the two modules through the use of six interconnecting wraparounds, epoxy-mounting the potentiometer and crystal assemblies to the VCXO submodule, and encapsulating the mated submodules in a molded shell to produce the finished device. This is not the final version, since it is intended that future devices will use ceramic packaged crystals only, and that the crystals will be incorporated within the VCXO submodule.

It was expected originally that this would necessitate the relocation of the regular circuit outside of the VCXO submodule, presumably in a separate enclosure, with an attendant increase in cost and complexity. However, the recommendations set forth in this section should allow crystal mounting within the VCXO submodule without requiring a separate package for the regulator. Additionally, the ability to pretest and adjust the oscillator with the crystal permanently emplaced, and with short connections unaffected by subsequent module potting, should greatly reduce processing time and result in vastly improved yields. The problems of pad lifting due to repeated soldering and unsoldering of crystal leads during various stages of processing will be eliminated, as will the thermal offset due to the separation between the crystal and the temperature sensor.

## 8.2 Proposed Objective

The purpose of this section is to recommend a redesign effort which will involve the following:

- a. Revise layout to allow both voltage regulator and crystal to be incorporated within the existing two modules.
- b. Reduce the total number of components and substitute lower cost components.
- c. Revise layout to allow for automated wire bonding.
- d. Revise layout to achieve easier testing at preseat and functional trimming.
- e. Use a precision thin-film resistor network to eliminate four presently required functional trims.
- f. Add a screening step using a high adhesion conducting paste (e.g., Raytheon's RQ<sub>1</sub>) to improve adhesion of soldering pads to the substrate and to permit rework without pad lifting failures.
- g. Redesign and evaluate electrical configurations to improve circuit performance.

The final objective is to reduce component and manufacturing labor costs; to increase manufacturing yields and improve module producibility; to enhance end product function and improve reliability.

### 8.3 Proposed Layout Changes

#### 8.3.1 Simplified TCFG Circuit

The TCFG circuit illustrated in Figure 8.1 can be replaced by the simplified circuit shown in Figure 8.2. The number of resistors is reduced from 60 to 44. Further modifications may produce additional reductions in resistor count. Circuit function and performance are unchanged, and the reduction of network nodes and in resistor count will simplify passive trimming. Presumably, only a single set-up will be required rather than the two presently needed, since the reduction in the number of necessary probes will allow the network to be trimmed in a single pass.

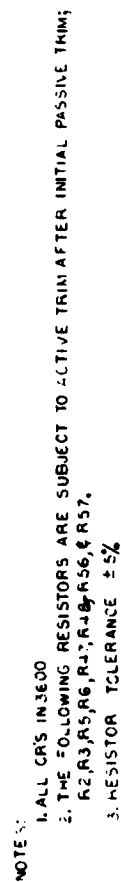
The major gain in available substrate area achieved by allowing the transfer of some circuit elements from the VCXO to the TCFG module will make it possible to place the crystal inside the VCXO submodule.

#### 8.3.2 Relocation of "U5" to the TCFG Submodule

The circuit should be repartitioned as shown in Figure 8.3, transferring U5 and its associated components to the TCFG module. This, combined with the changes detailed in Paragraph 8.3.1, will make enough area available within the VCXO module to permit internal mounting of the crystal without requiring an additional module for displaced components. Additional area will be freed by reducing the number of wrap-arounds from 6 to 5, and by eliminating the run connecting the crystal to pins 8 and 9 of the plug-in strip. In fact, since these pins no longer serve any functional purpose, they could be eliminated altogether, making additional space available on the substrate for other purposes.

#### 8.3.3 Thin-Film Resistor Network

Certain selected resistor groups should be combined into a thin-film network on a single chip with value, tolerance, and ratio tolerances as shown in Table 8.1.



**Figure 8.1 Original TCFG Circuit**

104



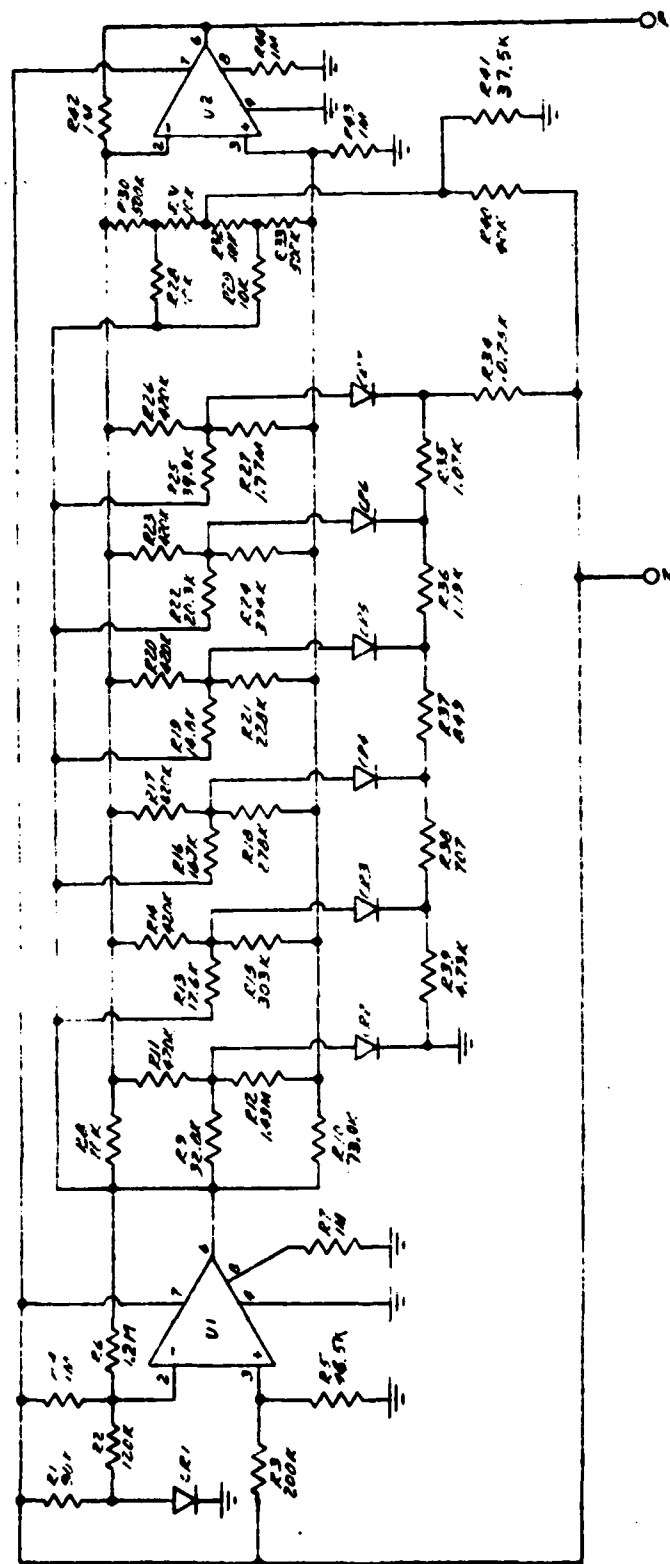
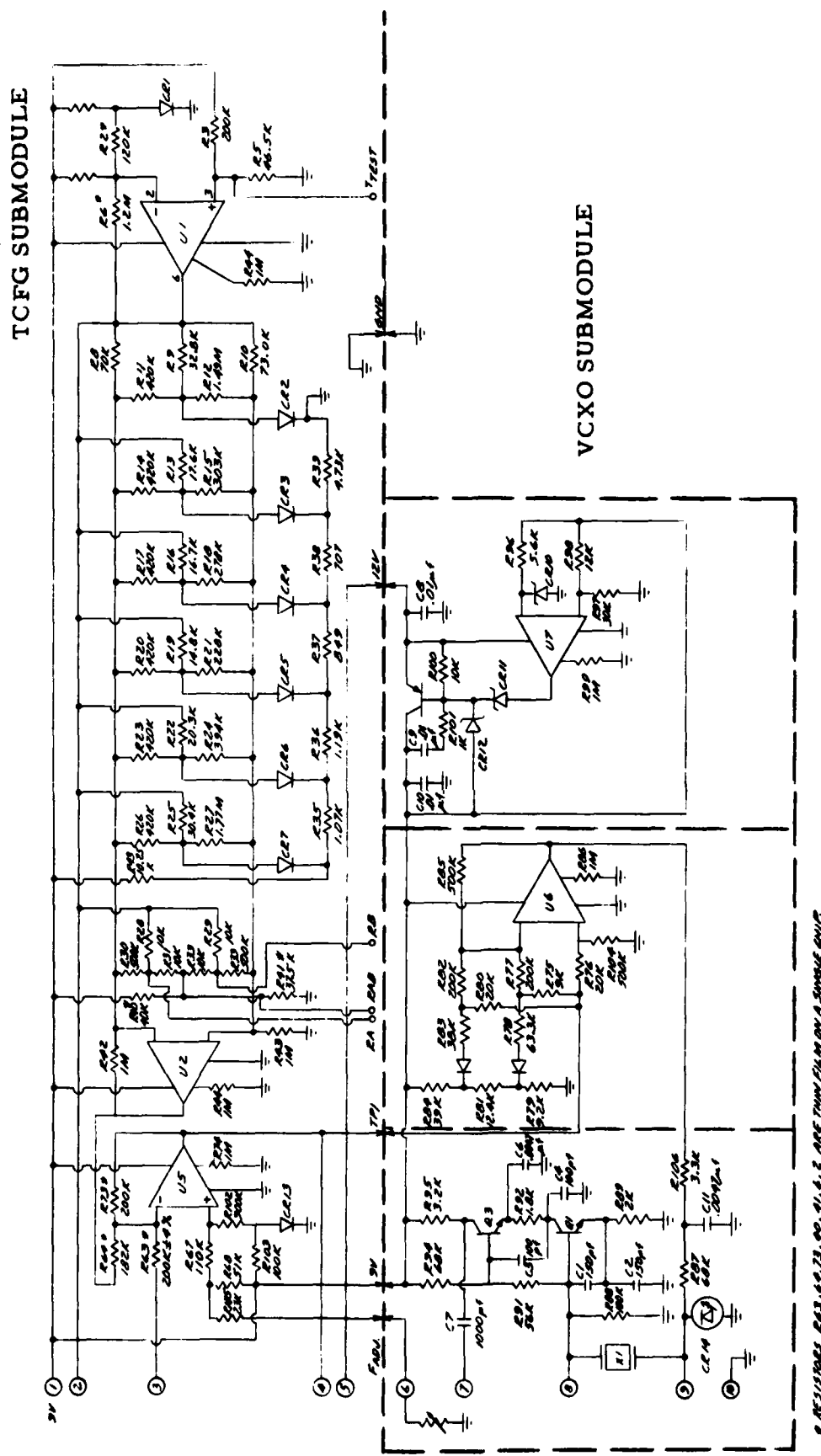


Figure 8.2 Simplified TCFG Circuit



**Figure 8.3 Circuit Partitioning; Redesign Schematic**

TABLE 8.1 THIN-FILM RESISTOR SPECIFICATIONS

<u>Res. No.</u>	<u>Value</u>	<u>Tolerance</u>	<u>Ratio Function</u>	<u>Ratio Tolerance</u>
R2	100K	5%		
R6	1 Meg	5%	$R6/R2 = 10$	0.1%
R63	200K	5%	$R73/R63 = 1$	0.1%
R64	182K	5%	$R73/R64 = 1.1$	0.1%
R73	200K	5%		
R56	32K	5%		
R57	30K	5%	$R56/R57 = 1.067$	0.1%

This is feasible because the relocation of U5 will bring all of the resistors specified to the TCFG module. Aside from the reduction in space required for the resistors, this will eliminate the need for the following active trims:

- a. Modulation gain
- b. Compensation gain
- c. Thermal gain
- d. TCFG rotation

The reduction in laser time required for active trim will allow greater volume thru-put in the line. Active trim, while required to custom tailor the devices to the crystal and to other active components within the circuit, is one of the major factors in volume production.

#### 8.3.4 Resistor Screening

The resistor geometries and patterns should be modified to:

- a. Reduce the number of resistor screenings from four to three on each module.
- b. Form all resistors requiring active trim into two parts, nominally 80% and 20% of the total value, to permit better control of variables during active trim. The 80% section would be passively trimmed, leaving the untouched 20% section available for active trimming.

#### 8.3.5 Conductor Screening

The conductor patterns should be modified to:

- a. Add test points.

The repartitioning of the circuit with the accompanying reduction of wraparounds will also permit all test and trim points to be brought to the edge of the substrate, external to the corral. This will eliminate the need to probe inside the corral during preseat testing and active trim, and will allow better diagnostics on the sealed modules. Refixturing the test and trim jigs to replace the probes with substrate edge connectors will speed handling and decrease yield loss due to probe damage.

At ERADCOM's request, the output of U1 can be brought out to pin 2 of the final module.

- b. Eliminate unnecessary runs to the crystal.
- c. Eliminate unneeded edge connector pins, specifically pins 8 and 9.
- d. Increase and reposition probe areas to optimize the patterns for passive trimming.
- e. Rearrange semiconductor bonding pads to permit the institution of automatic wire bonding.

#### 8.3.6 Reduction of Corral Length

The layout should be modified so that the length of the corral can be reduced by 0.020 inch to permit the wraparounds to be more easily attached and to create a more reliable connection.

#### 8.3.7 Hi "Q" Capacitors

The layout will be modified to permit C1 and C2 to be single 150 pf capacitors, rather than paralleled 75 pf capacitors as in the present design. These capacitors are Hi Q porcelain capacitors with a temperature characteristic of +90 ppm/degree C and a dissipation factor of 0.01%.

Because the unit cost for the porcelain capacitors is about eight times that of the other capacitors in the circuit, the necessity for such High Q components should be re-evaluated since C<sub>2</sub> is shunted with a low value resistor which, in effect, negates the High Q characteristic of the capacitor.

#### 8.4 Physical and Mechanical Changes (Not Involving Layout)

##### 8.4.1 Package Sealing

Sealing the package now involves the attachment of a Kovar frame via a preform to the top of the metallized corral, placing a gold-tin preform on the frame, and seam brazing the cover to the assembly. Three alternate methods are proposed.

Method #1 will replace the existing metallized corral with an unmetallized corral and replace the gold-plated Kovar cover with a nickel-plated Kovar cover. The unit will be sealed using an epoxy preform instead of the present weld seal.

Raytheon Quincy has successfully used epoxy preforms to cement ceramic covers to corrals approximately 1/4" x 1/2". For larger modules, Raytheon recommends the use of preforms made from Ablefilm 529. In the method proposed, the cover is made of nickel-plated Kovar, with a small pretinned opening to remove the pressure during curing. This opening is then reflow-soldered without flux in a dry nitrogen environment to form the final seal. ERADCOM lists two types of polymers in

Document SM-A779786 for sealing purposes. The specific epoxy to be used will be evaluated for effectiveness and compatibility with materials and components of the TCVCXO.

Method #2 will modify the metallization on the corral to permit the cover to be seam-brazed directly to the corral without the addition of the frame and initial preform.

Method #3 utilizes the technique of cluster sealing. In cluster-seal packaging, the active devices are arranged on the substrate in such a fashion that individual covers can be used to hermetically seal selected locations. An additional screening of low-temperature glass provides the seal rings for the cluster covers. These seal rings are fired to fuse the glass to the substrate at a temperature lower than the devitrification temperature of the glass. The substrates can then be processed through passive trim, die attach, wire bond, and active trim prior to sealing. Ceramic caps are preheated and pressed into position on the glass rings, reflowing the glass and forming the hermetic seal. The caps would take the place of the corral presently being used.

#### 8.4.2 New Potentiometer Assembly

The present potentiometer assembly is a costly and labor-consuming device. A suitably sealed potentiometer capable of attachment to the module without additional modification should be procured. It is felt that the potentiometer presently in use (which is qualified and tested to MIL-R-27208, including moisture resistance testing to MIL-STD-202) is usable without further modifications. The large number of potentiometer failures in various stages of processing under the present manufacturing procedure suggest that the modifications intended to improve moisture resistance actually dilute the reliability of the component.

#### 8.4.3 One Piece Encapsulation

The present encapsulation procedure involves placing the unit in a purchased potting shell, fitting a lid to the shell and unit, and then filling the module with encapsulant. The existing design has test points brought out through the back end of the shell. This requires precoating the assembly with RTV to prevent potting material from leaking through the back and sticking to the substrates. If test points are eliminated from the final configuration, this step can be omitted. If test points are still required, they could be routed to pins 8 and 9 of the plug-in strip, which serve no function at this time. Back access would no longer be required, and test points would be available right at the socket, with obvious advantages. If a meniscus could be tolerated, the unit could be filled with epoxy to the top of the opening of the shell, and the lid could be eliminated.

#### 8.4.4 Wraparounds

Reducing the length of the corrals (Section 4.6) allows the depth of the five edge terminals for the wraparounds to be increased. A tooled web of five clips spaced at 0.100 inch on center can be attached easily to perform the required substrate interconnections. This will leave adequate area to provide four test points (0.080 inch on center) on the TCFG side and one test point on the VCXO side, external to the corral (see redesign schematic - Figure 8.3).

Reinforcement of wraparound solder pads through the use of a special high-adhesion conductive paste should reduce the losses due to pad lifting and leaching arising from rework operations.

#### 8.5 Semi-Automatic Assembly and Test

Producing circuits at a rate of 500 per week requires that certain parts of the manufacturing process be semi-automated to achieve the necessary thru-put.



#### 8.5.1 Automatic Wire Bonding

Automatic wire bonding would increase production rate in the wire bond area. This would require some layout changes and the rearrangement of bonding pads.

#### 8.5.2 Chip Sealed Carriers

The use of chip sealed carriers would allow the concentration of all active components within sealed, pretestable assemblies. Wire bonding on the substrate would be eliminated. This scheme is compatible with automatic assembly techniques the attendant layout changes would probably eliminate the costly corral approach, while the ability to pretest all active components for all parameters, not just dc characteristics, would greatly improve finished product yields.

#### 8.5.3 Closed Loop Operation of the ESI Laser

Full closed loop operation of the ESI laser for active trim will be instituted to obtain the required rate. With the thin-film networks (Section 8.3.3) eliminating four of the trims presently being done, plus the resistor modifications (Section 8.3.4) permitting better control, this can readily be achieved. It will require new active trim programs for both the TCFG and the VCXO sides.

Module inputs and outputs will interface with the laser computer for control and calculation. The trimming of the repartitioned circuit can be accomplished per Table 8.2. Equipment required for this is as follows.

- a. Digital thermometer
- b. Digital dc voltmeter/ohmmeter
- c. Digital controlled power supply
- d. Frequency counter

TABLE 8-2 - ACTIVE TRIM - SCHEMATIC FIGURE 8.3

TCFG

<u>Function</u>	<u>Input</u>	<u>Trim</u>	<u>Output</u>
Thermal Ref.	Temperature	R3/R5	DC Volts (Pin 2)
XTAL Compensation	Resis. Value	R31/R32	Ohms

VCXO

Volt Reg.		R97/R98	DC Volts (9 V)
Lin Level	1.5 VDC (TP1)	R76/R104	DC Volts (Eo)
Fo	1.5 VDC (TP1)		Freq. (Pin 7)
$\Delta F1$	3.5 VDC (TP1)	R75/R78	$\Delta$ Freq. (Pin 7)
$\Delta FZ$	4.5 VDC (TP1)	R80/R83	$\Delta$ Freq. (Pin 7)

Note: If circuit modifications dictate more breaks in the linearization network, additional  $\Delta F$  trims will be performed.

#### 8.5.4 Temperature Aging

At a delivery rate of 500 circuits per week, the lot sampling plan as specified in MIL-O-55310A (inspection level S-4, AQL 1%) would require a sample size of 50 pieces if a MAN of one was used.

Over an eight week stabilization period, this would mean that 400 aging sockets would be required with 400 frequency readings per day taken, compiled and compared.

The equipment required for this would be grouped in three areas and would consist of the following:

a. Main station

Rubidium standard  
Frequency synthesizer GR 1061  
Controller 9825A  
23 KByte memory  
Disc storage 9885M  
Slave disc 9885S

b. Movable rack

Frequency counter HP 5345  
Scanner (80 position) HP 3495X2

c. Aging chambers (5 required)

80 Module bath blue M MW1240A-1  
Wiring per bath

#### 8.5.5 Automatic Testing

Automatic testing of the final modules should include storing temperature run data in disc memory and generating temperature curves off line. The present method (Figure 8.4) of multiplexing recorders is definitely a gating factor in manufacture and would create a sizeable hardware problem at higher volume production. An automatic testing system similar to that shown in Figure 8.5 is needed.

The automatic testing system would require the following components:

- 1 - HP Quartz Thermometer Model 2804A with 2 laboratory probes
- 1 - Sigma Systems Oven Model 100 with microprocessor controller
- 1 - HP Automatic Data Acquisition System Model 3052A W/option 3437A deleted
- 1 - 20 Channel Scanner Model HP 3495 with 2 options 001
- 1 - HP Calculator 9825A with 23K bytes memory
- 4 - Dual VHF Switches Model 2804A
- 1 - HP Digital Voltmeter Model 3455B
- 1 - HP Power Meter Model 436A with option 22
- 1 - HP Power Supply Model 6131C
- 1 - HP Power Supply Model 6002A
- 1 - Data Control Systems Discriminator W/HP1B
- 1 - HP Counter Model 5345A
- 1 - HP Flexible Disc Drive Model 9883
- 1 - HP XY Plotter Model 9872A
- 1 - HP Printer Model 6002A

The required specifications to have the equipment vendor or a qualified source create the necessary software to implement all of the required testing functions will be generated.

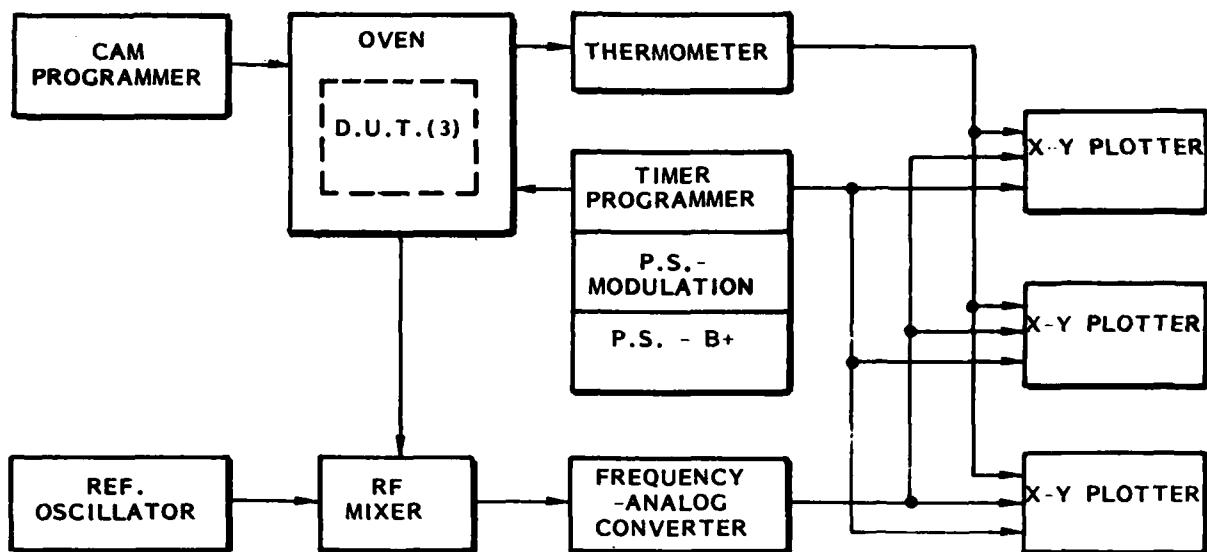


Figure 8.4 Multiplex Frequency Temp. Test Set-up

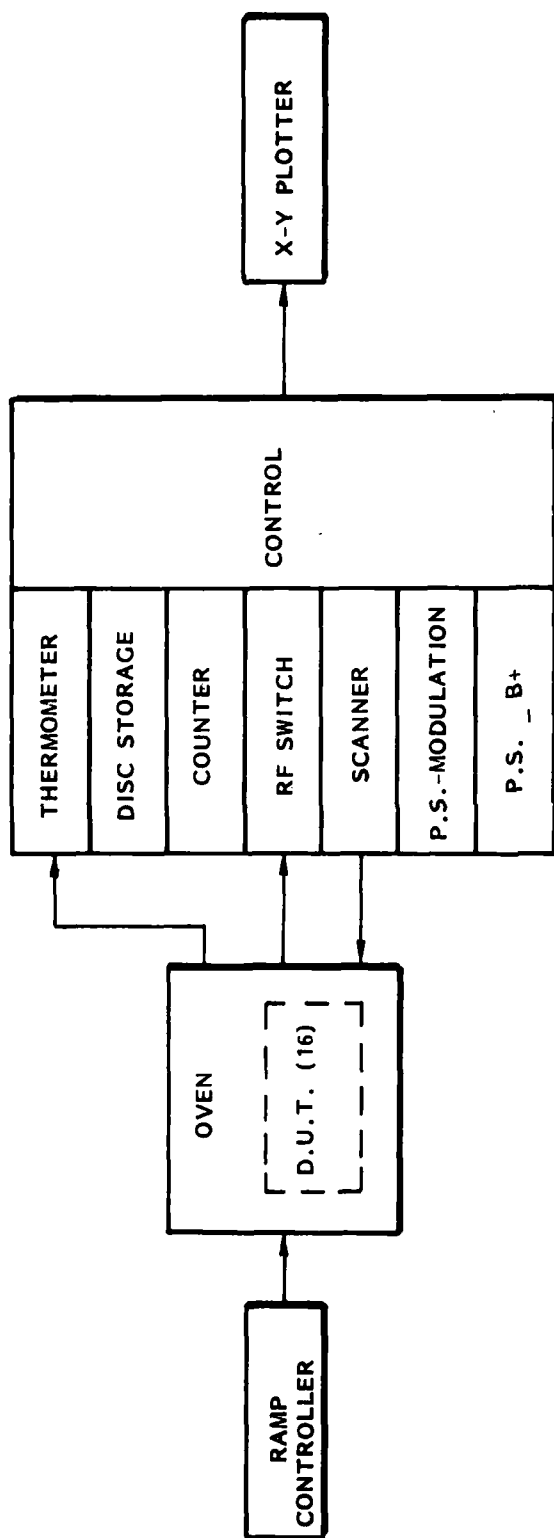


Figure 8.5 Proposed Automatic Frequency - Temperature Test System

## 8.6 Circuit Redesign

The proposed circuit redesign primarily covers two main areas.

### 8.6.1 TCFG Redesign

Basically, the TCFG redesign will incorporate the changes indicated in Section 8.3.1. However, the modifications will have to be evaluated using computer-aided design analysis to verify the validity of the design and investigate the sensitivity of the transfer function to resistor value changes. This will allow proper tolerancing of the circuit.

### 8.6.2 VCXO Redesign

The VCXO redesign is intended to improve the frequency deviation characteristics of the module under all operating conditions, with primary emphasis on the frequency deviation vs temperature behavior of the circuit. Coupled with this will be an investigation of the trim procedure required to obtain the optimum characteristic desired in the final units. Computer-aided design will be used to create a model of the crystal oscillator and varactor to the best voltage forcing function required.

The diode linearization function generator will then be modified to implement this function. Since the two segment DFG presently used does not offer a wide enough performance margin, the use of a four or five segment DFG is under consideration.

The final configuration will also be subjected to CAD to verify the validity of the design and to determine the sensitivity of the transfer function to temperature and components variations. The final design will then be characterized and toleranced.

The voltage regulator will also undergo computer analysis to eliminate the high limit voltage regulation failures encountered from time to time. The final design will incorporate the changes suggested by this investigation.

#### **8.6.3     Computer-Aided Design**

The form of CAD to be used in the redesign consists of integrated families of computer programs which will perform the following functions:

- a. DC Analysis to establish operating point centers and sensitivity of the output functions to particular part parameter. The determination of extreme tolerance limits of the components parameters and analysis of failure probability from tolerance build-up.
- b. AC Analysis to provide sinusoidal response and sensitivity of the configuration and to determine the tolerance requirements of components affecting the ac parameters of the circuit.
- c. Transient Analysis for evaluation of transient turn-on and turn-off characteristics of the system.
- d. Parameter Model Generation to provide accurate representations of the active components designed into the system.

Some program families that can perform the above functions are:

RAYCAD  
ECAP  
CIRCUS  
SCEPTRE  
NET I

The specific program to be used will be determined.



### SAVINGS SUMMARY

	Present Design Should Cost	New Design Should Cost
Labor Utilization	80%	80%
Substrate Yield	72.3%	81%
Assembly Yield	80%	85%
Chip Yield	82%	87%
Yielded Material	\$60.94	\$32.11
Yielded Touch Labor	19.56	11.77
Support Labor	4.68	2.64
TOTAL COST LEVEL	\$167.95	\$93.99

NOTE: (a) All labor costs are based on September 1978 rates.

APPENDIX A  
ELECTRONICS COMMAND  
TECHNICAL REQUIREMENTS  
SCS-483

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OSCILLATOR, CRYSTAL, TEMPERATURE COMPENSATED VOLTAGE  
CONTROLLED (TCVCXO) 17MHz to 22 MHz HERMETIC SEAL.

1. SCOPE

1.1 Scope.-- This specification covers the detailed requirements for a  $\pm 5$  ppm overall frequency tolerance temperature compensated voltage controlled crystal oscillator (TCVCXO).

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue in effect on the date of invitation for bid, forms a part of this specification to the extent specified herein.

SPECIFICATION

MIL-M-38510	Microcircuits, General Specification.
MIL-O-55310	Oscillators, Crystal, General Specification For.
SCS-463	Shock Resistant Crystal Units.

STANDARDS

MIL-STD-202	Test Methods for Electronic and Electrical Component Parts.
MIL-STD-883	Test Methods and Procedures for Microelectronics.

(Copies of specifications required by contractors in connection with specific procurement functions may be obtained from or as directed by the contracting officer. Both titles and identifying number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 General.-- The complete requirements for the crystal oscillator described herein shall consist of this document and the latest issue of specification MIL-O-55310.

3.2 Electrical.-- The TCVCXO shall be consistent with the functional block diagram and schematics, Figure 1 and 2 respectively. The TCVCXO shall operate at antiresonance and not include inductors. Linearization of the VCXO frequency-voltage tuning characteristic shall be obtained by means of a diode function generator (DFG) which produces a piecewise linear approximation of the linearizing voltage transfer function. Frequency-temperature (F-T) compensation shall be obtained with a similar DFG which generates a cubic transfer function approximating the characteristic of the uncompensated VCXO. The compensating DFG shall also incorporate a capability for rotating the DFG cubic transfer characteristic to correct for deviation of the crystal unit F-T characteristic from the design center curve. Provision (not included in Figure 2) shall also be made for adjusting the compensating characteristic to accommodate the range of frequencies given in 3.9.

3.3 Microcircuit Design and Construction.-- Microcircuit design and construction shall be in accordance with paragraph 3.5 of MIL-M-38510 and specified herein. Thick film hybrid circuitry shall be employed. The number of bonded interconnections shall be minimized by employing multiple layer conductors with dielectric crossovers. Leads and bonds shall be confined to interconnections with the semiconductor devices. Beam leaded devices shall be used wherever possible. Maximum length of interconnecting leads shall be 0.050 inches and leads shall not cross over uninsulated conductors.

3.4 Film Resistor Trimming.-- Passive and active resistor trimming shall be accomplished using a resistance laser trim system.

3.5 Package.-- The package shall be a multiple pin enclosure having a volume not exceeding 0.45 cubic inches (TEKFORM, FSCM 29172, Parts #20269 and #20270 or equivalent).

3.6 Quartz Crystal.-- Quartz crystal unit CR-(XM-159)/U in accordance with SCS-463 shall be employed in the TCVCXO.

3.7 Seal.-- The TCVCXO shall be sealed in an atmosphere of dry helium or nitrogen. Maximum leak rate shall be  $1 \times 10^{-8}$  atm cc/sec. (See 4.7).

3.8 Weight.-- The maximum weight shall be 20 grams. (See 4.3).

3.9 Frequency Range.-- The frequency range of the TCVCXO shall be 17 MHz to 22 MHz. (See 4.3).

3.10 Frequency-Temperature Stability.— The frequency change of the TCVCXO shall not exceed  $\pm 2$  ppm over the range of  $-40^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$  at center frequency and at frequency deviation limits of  $\pm (375/F + 3)$  ppm where F is the nominal frequency in MHz. (See 4.8).

3.11 Frequency-Voltage Stability.— The frequency change for a power supply variation given in 3.22 shall not exceed  $\pm 0.25$  ppm. (See 4.3).

3.12 Frequency-Load Stability.— The frequency change for an output termination resistance change of  $\pm 20\%$  shall not exceed  $\pm 0.25$  ppm. (See 4.3).

3.13 Transient Frequency Stability (initial turn on).— The transient frequency shift between the first 5 msec to 100 msec following application of power shall be less than 6 Hz. (See 4.3).

3.14 Aging.— The frequency aging at  $60^{\circ}\text{C} \pm 0.1^{\circ}\text{C}$  shall not exceed  $1 \times 10^{-8}$  over any one week interval following a 14 day stabilization period at  $60^{\circ}\text{C}$ . (See 4.9).

3.15 Shock.— The frequency change following a 1000g, 6 millisecond shock shall be less than  $\pm 0.5$  ppm. (See 4.10).

3.16 Vibration.— The difference between TCVCXO frequency measured before and after vibration at 0.06" double amplitude, 10 to 70 Hz and at constant 15g from 70 Hz to 2000 Hz shall be less than  $\pm 0.5$  ppm. (See 4.11).

3.17 Frequency Adjustment.— Frequency adjustment shall be accomplished external to the TCVCXO by means of a 25K ohm potentiometer. The minimum frequency adjustment range shall be  $\pm 5$  ppm of the nominal frequency. (See 4.12).

3.18 Modulation Input Voltage.— The magnitude of the applied modulation voltage shall be  $1.5\text{V} \pm 0.01\text{V}$  peak to peak for a 300 bit per second square wave (FSK) or  $1.5\text{V} \pm 0.01\text{V}$  peak to peak (DC to 2000 Hz) sine wave (analog). The dc level is  $0.0\text{V} \pm 0.01\text{V}$ . (See 4.13).

3.19 Modulation Input Impedance.— The modulation input impedance shall be 200K ohms  $\pm 10\%$ . (See 4.14).

3.20 Frequency Deviation.— The modulation deviation of the TCVCXO corresponding to the peak to peak modulation input voltages of 3.18 shall be  $\pm 375$  Hz  $\pm 5\%$  of center frequency. (See 4.15).

3.21 Deviation Linearity.— The deviation linearity of the TCVCXO shall be less than 1%. (See 4.16).

3.22 Supply Voltages.-  $+9V \pm 0.01V$  dc,  $-9V \pm 0.01V$  dc. (See 4.17).

3.23 Inout Power.- 85mW maximum. (See 4.18).

3.24 Output Voltage.- The RF output voltage shall be not less than 80mV rms when loaded by  $50 \text{ ohm} \pm 10\%$ . (See 4.19).

3.25 Marking.- The TCVCXO shall be marked with index point, serial number, manufacturers code designation, week and year of manufacture and calibration  $\Delta F$  offset at  $30^\circ \pm 1^\circ\text{C}$  as a minimum. (See 4.20).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection.- The contractor is responsible for the performance of all inspections specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the Government. Inspection records of the examinations and tests shall be kept complete and available to the Government as specified in the contract.

4.2 Classification of inspection.- Inspection shall be classified as follows:

(a) First article inspection (does not include preparation for delivery). (See 4.4).

(b) Quality conformance inspection. (See 4.5).

4.3 Test plan.- The contractor prepared Government-approved test plan as cited in the contract shall contain:

(a) Time schedule and sequence of examinations and tests.

(b) A description of the method of test and procedures.

(c) Programs of any automatic tests including flow charts and block diagrams.

(d) Identification and brief description of each inspection instrument with date of most recent calibration.

4.4 First article inspection.- This inspection shall consist of all the tests contained in Table II of MIL-O-55310 and as specified below. No failures shall be permitted.

4.5 Quality conformance inspection.- This inspection shall be performed on samples selected from the pilot production as specified in the bid request and contract. Quality conformance inspection shall be conducted in accordance with Paragraph 4.7 of MIL-O-55310 and as specified below.

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4.6 Screening.- Prior to first article and quality conformance inspection, each TCVCXO shall have been screened according to method 5004.1, "Screening Procedures", Class B, MIL-STD-883 except for 3.1.5 mechanical shock, 3.1.6 constant acceleration and 3.1.7 seal. Qualification or quality conformance inspection, 3.1.14 of the screening tests, shall be limited to the high temperature storage test, Group C, subgroup 4 of method 5005.1.

4.7 Seal.- The TCVCXO shall be tested in accordance with Test Condition C, Procedure IV, Method 112A of MIL-STD-202D.

4.8 Frequency-Temperature Stability.- The TCVCXO shall be tested in accordance with 4.8.8.1 of MIL-O-55310.

4.9 Aging.- The aging shall be tested in accordance with 4.8.29 of MIL-O-55310. Continuous measurement period 8 weeks; measurement interval 24 hrs.

4.10 Shock.- Shock performance shall be tested in accordance with Condition E, Method 213A of MIL-STD-202D except shock duration shall be 6 milliseconds.

4.11 Vibration.- Vibration performance shall be tested in accordance with Condition B, Method 204B of MIL-STD-202D.

4.12 Frequency Adjustment.- The frequency adjustment range shall be tested in accordance with 4.8.9 of MIL-O-55310.

4.13 Modulation Input Voltage.- The modulation input voltage shall be tested in accordance with 4.8.4.3 of MIL-O-55310.

4.14 Modulation Input Impedance.- The modulation input impedance shall be tested in accordance with 4.8.5 of MIL-O-55310.

4.15 Frequency Deviation.- The frequency deviation shall be tested in accordance with 4.8.25 of MIL-O-55310.

4.16 Deviation Linearity.- The deviation linearity shall be tested in accordance with 4.8.27 of MIL-O-55310.

4.17 Supply Voltage.- The supply voltage shall be tested in accordance with 4.8.4.1 of MIL-O-55310.

4.18 Input Power.- The input power shall be tested in accordance with 4.8.6.1 of MIL-O-55310.

4.19 Output Voltage.- The output voltage shall be tested in accordance with 4.8.12.1 of MIL-O-55310.

4.20 Marking.- Marking shall be in accordance with 3.6 of MIL-O-55310.

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5. PREPARATION FOR DELIVERY

5.1 Preparation for Delivery.- Preparation for delivery shall be as specified in the contract.

6. NOTES

6.1 Overall Frequency Tolerance.- The intended application for this device requires that the frequency remain within  $\pm 5$  ppm from nominal frequency under any combination of environment and input voltage conditions contained herein and over a period of 1 year following initial calibration.



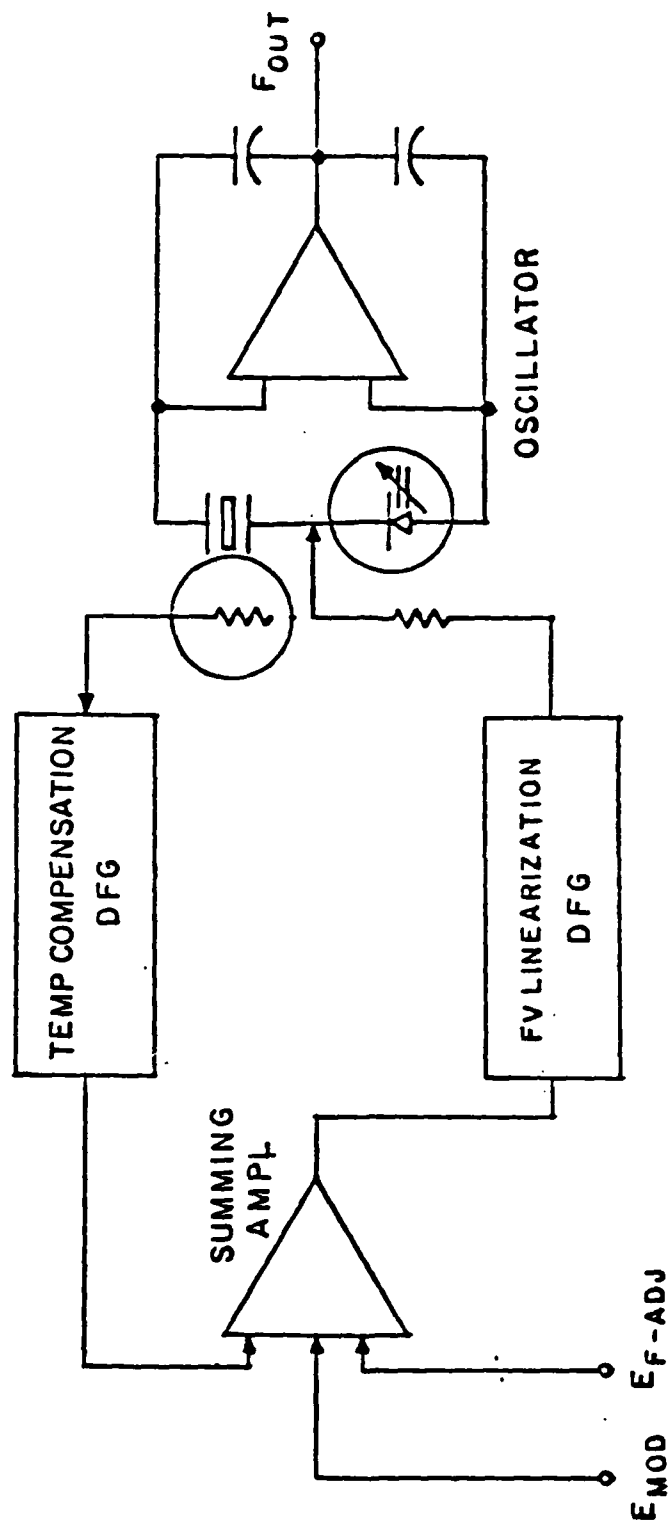


FIG 1 TCVCXO BLOCK DIAGRAM



OSCILLATOR, CRYSTAL, TEMPERATURE COMPENSATED  
VOLTAGE CONTROLLED (TCVCXD) 17 MHz to 22 MHz  
HERMETIC SEAL

This amendment forms a part of Electronics Command Technical Requirements SCS-483  
17 January 1975

Page 1

2.1 Delete title heading "SPECIFICATION" and substitute "SPECIFICATIONS"

Under SPECIFICATIONS delete "SCS-463" and substitute "SCS-512"

Page 2

3.3 Add following sentence to end of paragraph: "Epoxy adhesives shall be permitted for mechanical attachment of IC devices within the hermetic enclosures."

3.5 delete and substitute:

"3.5 Package.-- The TCVCXD package shall be in accordance with outline and assembly drawings Figures 3 and 4 respectively."

3.6 delete "SCS-463" and substitute "SCS-512".

3.7 delete and substitute:

"3.7 Seal.-- The TCVCXD assembly, without encapsulation, shall be sealed in an atmosphere of dry helium or nitrogen. Maximum leak rate shall be  $1 \times 10^{-6}$  atm cc/sec. (See 4.7)."

3.8 delete "20 grams" and substitute "30 grams".

Page 3

3.10 delete "(375/F+3)ppm" and substitute "(325/F+5)ppm".

3.13 delete "6 Hz" and substitute "10 Hz".

3.16 delete "+ 0.5 ppm" and substitute "+ 0.25 ppm".

3.17 delete "external to the TCVCXD".

SCS-483  
AMENDMENT-3

3.18 delete and substitute:

"3.18 Modulation input voltage.- The modulation input voltage shall be defined as follows:

Digital modulation (FSK): SPACE-logic zero, MARK-logic one (5 V positive), CMOS inverter input.

Digital modulation rate: FSK of 1200 data bits per second.

Analog modulation voltage:  $\pm 0.75$  V peak max.

Analog modulation rate: DC to 10 kHz max.

Analog transmission control: Analog transmit +5  $\pm$  1 VDC,  
Digital transmit 0 to +1 VDC. (see 4.13)."

3.19 delete and substitute:

"3.19 Analog modulation input impedance.- The analog modulation input impedance shall be  $\geq 200,000$  ohms. (see 4.14)."

3.20 delete and substitute:

"3.20 Frequency deviation.- The FSK frequency deviation from center frequency shall be +300 Hz to +325 Hz for MARK and -300 Hz to -325 Hz for SPACE. Analog frequency deviation sensitivity shall be 500 Hz per volt. (see 4.15)."

3.21 delete and substitute:

"3.21 Analog deviation linearity.- The analog deviation linearity shall be less than 5%. (see 4.16)."

Page 4

3.22 delete and substitute:

"3.22 Supply voltage.- +10 VDC min to +15 VDC max, nominal +12 VDC. (see 4.17)."

3.23 delete and substitute:

"3.23 Input power.- 50 mW maximum. (see 4.18)."

3.24 delete and substitute:

"3.24 Output voltage.- The RF output voltage shall be not less than 0.5 V rms when loaded by 1000 ohms  $\pm$  10%. (see 4.19)."

Page 8

Fig 2, delete present Fig 2 and substitute new Fig 2, "REMBASS TCVCXO SCHEMATIC"

Page 9

add Page 9, Fig 3, "TCVCXO MODULE OUTLINE DRAWING"

Page 10

add Page 10, Fig 4, "TCVCXO MODULE ASSEMBLY"

11-5004

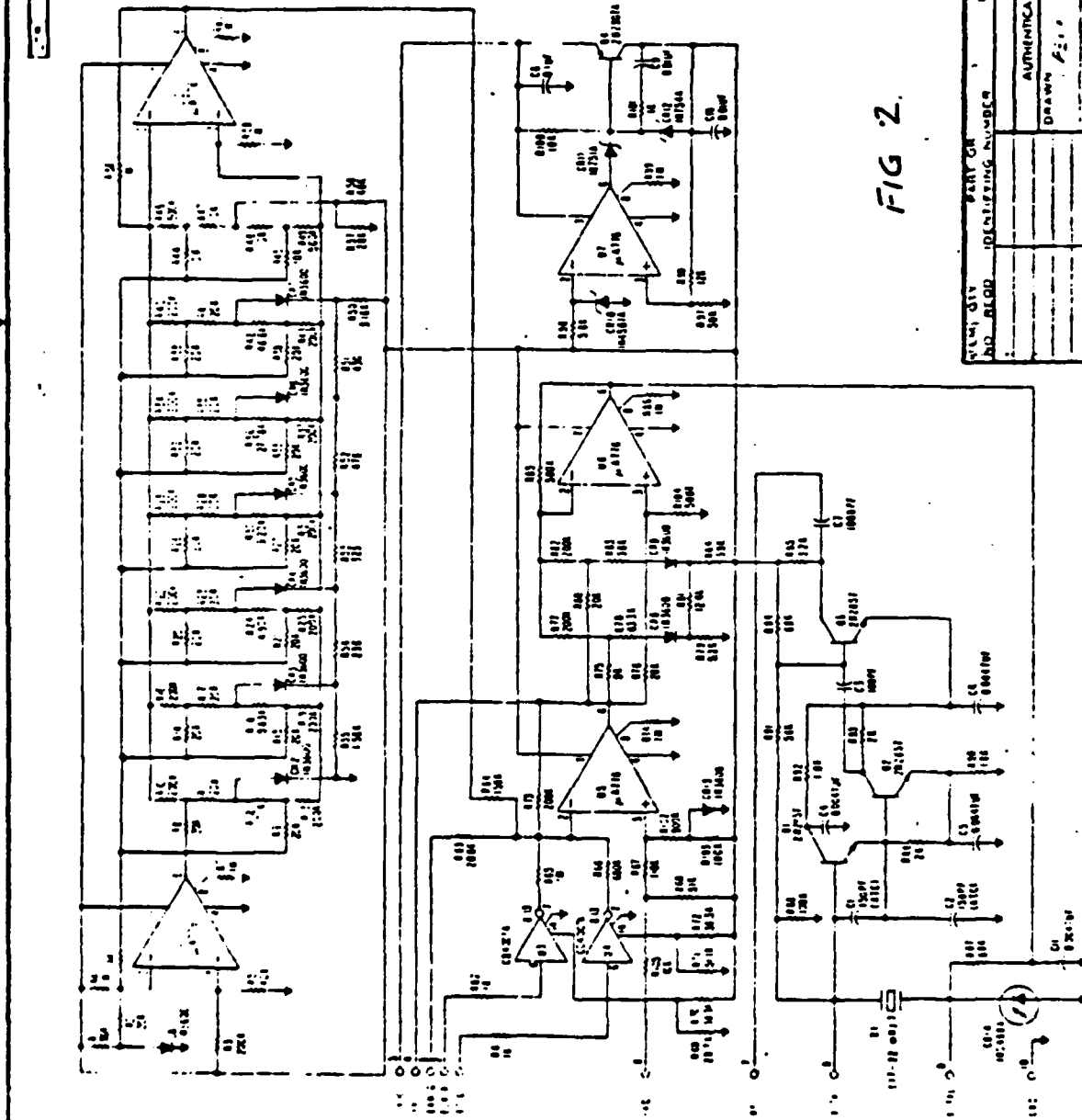


FIG 2.

VIEW, QTY	IDENTIFYING NUMBER	NOMENCLATURE OR DESIGNATION	SPEC. NO.
AND RECD		PART 101	
AUTHENTICATION		REMBASS TVCAO SCHEMATIC	
DRAWN BY: <i>CHENYU</i>		DATE: <i>11-5-52</i>	
CHECKED BY: <i>VERITY</i>		DATE: <i>11-5-52</i>	
APPROVED BY: <i>VERITY</i>		DATE: <i>11-5-52</i>	
USED ON: <i>REMBASS TVCAO</i>		DATE: <i>11-5-52</i>	
APPLICATION: <i>REMBASS TVCAO</i>		DATE: <i>11-5-52</i>	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES			
C 20309		SCALE: <i>1:1</i>	



DOC-403  
AMENDMENT-3

REVISIONS  
DATE

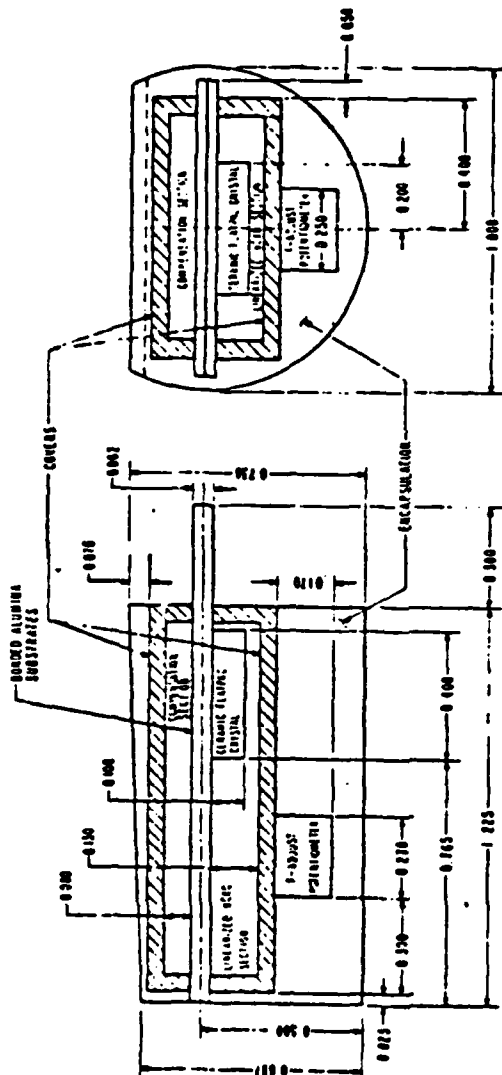


FIG. 4.

ITEM NO.	QTY.	PART OR IDENTIFYING NUMBER	DESCRIPTION	DATE				
100	1	TCVCXO MODULE ASSEMBLY	REVISED TO INCLUDE PHOTOGRAPHIC	10 OCT 75				
<table border="1"> <tr> <td>APPROVED</td> <td>DATE</td> </tr> <tr> <td>D. PEREIRA</td> <td>10 OCT 75</td> </tr> </table>					APPROVED	DATE	D. PEREIRA	10 OCT 75
APPROVED	DATE							
D. PEREIRA	10 OCT 75							
<table border="1"> <tr> <td>REVISIONS</td> <td>DATE</td> </tr> <tr> <td>1</td> <td>10 OCT 75</td> </tr> </table>					REVISIONS	DATE	1	10 OCT 75
REVISIONS	DATE							
1	10 OCT 75							
<table border="1"> <tr> <td>TCVCXO MODULE ASSEMBLY</td> </tr> <tr> <td>ES-C-212775</td> </tr> </table>					TCVCXO MODULE ASSEMBLY	ES-C-212775		
TCVCXO MODULE ASSEMBLY								
ES-C-212775								



★  
OSCILLATOR, CRYSTAL, TEMPERATURE COMPENSATED  
VOLTAGE CONTROLLED (TCVCXO) 21.9375 MHz  
HERMETIC SEAL

This amendment forms a part of Electronics Command Technical Requirements SCS-483  
17 January 1975

Page 1

★ TITLE delete "17 MHz to 22 MHz" and substitute "21.9375 MHz."

★ 1.1 line 2, delete "+ 5 ppm overall frequency tolerance."

★ Add new paragraph:

"1.2 Type designation: The following type designation shall apply:

<u>TCVCXO TYPE</u>	<u>OVERALL FREQUENCY TOLERANCE</u>	<u>CRYSTAL TYPE USED (SEE 3.6)</u>
TCVCXO-1	+10 ppm	METAL ENCLOSED
TCVCXO-2	+10 ppm	CERAMIC FLATPACK
TCVCXO-3	+30 ppm	CERAMIC FLATPACK "

2.1 Delete title heading "SPECIFICATION" and substitute "SPECIFICATIONS"

Under SPECIFICATIONS:

★ add "MIL-C-3098 Crystal Units, Quartz, General Specification For"

delete "SCS-463" and substitute "SCS-512"

Page 2

★ 3.2 delete last sentence, "Provision (not included in Figure 2) shall ... given in 3.9."

SCS-483  
AMENDMENT-4

3.3 delete and substitute:

"3.3 Microcircuit Design and Construction.- Microcircuit design and construction shall be in accordance with paragraph 3.5 of MIL-M-38510 and specified herein. Thick film hybrid circuitry shall be employed. The number of bonded interconnections shall be minimized by employing multiple layer conductors with dielectric crossovers. Maximum length of interconnecting leads shall be 0.050 inches and leads shall not cross over uninsulated conductors. Epoxy adhesives shall be permitted for mechanical attachment of IC devices within the hermetic enclosures."

3.5 delete and substitute:

"3.5 Package.- The TCVCXO package shall be in accordance with Raytheon outline drawing number 31865 and Raytheon module assembly drawing number 31380, or equivalent."

\* 3.6 delete and substitute:

"3.6 Quartz crystal.- Metal enclosed quartz crystal units used in the fabrication of the TCVCXO-1 type shall be in accordance with MIL-C-3098. Ceramic flat pack quartz crystal units used in the fabrication of TCVCXO-2 and -3 shall be in accordance with SCS-512."

\* 3.7 delete and substitute:

"3.7 Seal.- The TCVCXO microcircuit assemblies, without encapsulation, shall be sealed in an atmosphere of dry helium or nitrogen. Maximum leak rate shall be  $1 \times 10^{-8}$  atm cc/sec. (See 4.3)."

\* 3.8 delete "20 grams" and substitute "30 grams."

\* 3.9 delete and substitute:

"3.9 Center Frequency.- The nominal center frequency shall be 21.937500 MHz. Center frequency is defined as the output frequency which results when a d.c. voltage of 2.500V  $\pm 0.001$ V is present at the modulation input terminal of the TCVCXO."

- \* 3.10 delete and substitute:

"3.10 Frequency Temperature Stability.- The frequency change shall not exceed the values specified below over the temperature range of -40°C to 75°C at center frequency (see 3.9) and at specified Mark and Space deviation levels (see 3.20.1). (See 4.8)

<u>TYPE</u>	<u>F/T STABILITY</u>
TCVCXO-1	+5 ppm
TCVCXO-2	+5 ppm
TCVCXO-3	+25 ppm "

3.13 line 3, delete "6 Hz" and substitute "10 Hz."

- \* 3.14 line 1, delete "1X10<sup>-8</sup>" and substitute "1.25 ppm for the TCVCXO-1 and 2X10<sup>-8</sup> for the TCVCXO-2 and TCVCXO-3."
- \* 3.15 delete and substitute:

"3.15 Shock.- The maximum frequency change shall not exceed +0.5 ppm when subjected to shock at levels specified below. (See 4.10).

<u>TYPE</u>	<u>PEAK VALUE (g's)</u>	<u>DURATION (MS)</u>
TCVCXO-1	100	6
TCVCXO-2	1500	0.5
TCVCXO-3	1500	0.5 "

3.16 line 3, delete "+ 0.5 ppm" and substitute "+ 0.25 ppm."

- \* 3.17 delete and substitute:

"3.17 Frequency Adjustment Range.- The minimum frequency adjustment range shall be +5 ppm of the nominal center frequency. (See 4.12)."

SCS-483  
AMENDMENT-4

- \* 3.18 delete and substitute:

"3.18 Modulation Input Voltage (See 4.13).- The modulation input voltage shall be defined as follows:

Digital modulation (FSK):

+  $E_{\text{mod}}$  (SPACE) = 0.625 V +2%

-  $E_{\text{mod}}$  (MARK) = 0.625 V +2%

Digital modulation rate: FSK of 1200 bits/sec

Analog modulation voltage: 2.500 V  $\pm$ 0.750V peak, max.

Analog modulation rate: DC to 8 KHz max. "

- \* 3.19 delete and substitute:

"3.19 Modulation Input Impedance.- The modulation input impedance shall be 200,000 ohms  $\pm$ 5% (See 4.14)."

- \* 3.20 delete and substitute:

"3.20 Frequency Deviation.-

3.20.1 Digital (FSK).- The FSK frequency deviation from center frequency shall be  $\pm$ 312.5 Hz  $\pm$ 10% for MARK and  $\pm$ 312.5 Hz  $\pm$ 10% for SPACE. (See 4.15).

3.20.2 Analog.- Analog frequency deviation (deviation sensitivity) shall be 500 Hz per volt  $\pm$ 8%. (See 4.15)."

- \* 3.21 delete and substitute:

"3.21 Analog Deviation Linearity.- The analog deviation linearity shall be less than 5%. (See 4.16)."

Page 4

- \* 3.22 delete and substitute:

"3.22 Supply Voltage.- +10V DC min. to +16V DC max, nominal +12V DC. (See 4.17)."

\* 3.23 delete and substitute:

"3.23 Input Power.-- 48mW max at nominal +12V DC, 4.0 ma max at +16V DC, for no load condition at regulated 9V TCVCXO output. (See 4.18)."

\* 3.24 delete and substitute:

"3.24 Output voltage.--

3.24.1 RF Output.-- The RF output voltage shall not be less than 1.0 V peak to peak when loaded by 1000 ohms +10%. (See 4.19).

3.24.2 Regulated DC Output.-- The accuracy of the regulated DC output shall be 9.000 V +0.020 V over combined effects of specified temperature and supply voltage variation and load variation from no load to full load (1 ma max). (See 4.3)."

\* 3.25 delete and substitute:

"3.25 Marking.-- The TCVCXO shall be marked with type designation, serial number, manufacturers code, week and year of manufacture and calibration  $\Delta F$  offset at 30°  $\pm 1^\circ\text{C}$  as a minimum. (See 4.20)."

\* 4.4 delete and substitute:

"4.4 First Article Inspection.-- This inspection shall consist of all the tests contained in Table I of MIL-O-55310 (with the exception of the seal test), aging test (see 4.9), and Table II (Group 1 only) of MIL-O-55310, respectively, in the order shown. These tests shall be performed on all the sample units. No failures shall be permitted."

\* 4.5 delete and substitute:

"4.5 Quality conformance inspection.-- This inspection shall be performed on samples selected from the pilot production as specified in the bid request and contract. Quality conformance inspection shall be performed in accordance with paragraph 4.7 of MIL-O-55310 (with the exceptions that (a) the Seal test be deleted from Group A inspection (Table I) and (b) only the Group 1 tests of Group C inspection (Table II) shall be performed), and as specified below.

- \* 4.6 delete and substitute:

"4.6 Screening.- Each TCVCXO microcircuit subassembly shall be screened in accordance with Method 5008 of MIL-STD-883 with the following exceptions:

- (a) Bond Strength (para. 3.2.2.1) shall be performed on all first article units.
- (b) Temperature Cycling (para. 3.2.3.4) shall be performed in accordance with test condition B.
- (c) Mechanical Shock or Constant Acceleration (para. 3.2.3.5).- Constant acceleration only shall be performed.
- (d) Omit test procedures 3.2.1.1, 3.2.3.11, 3.2.3.12 and 3.2.3.13."

- \* 4.7 delete in its entirety.
- \* 4.9 line 1, delete "4.8.29" and substitute "4.8.31."
- \* 4.15 line 2, delete "4.8.25" and substitute "4.8.26."
- \* 4.16 line 2, delete "4.8.27" and substitute "4.8.28."
- \* 4.20 delete "3.8" and substitute "3.6."

- \* 6.1 delete and substitute:

"6.1 Overall Frequency Tolerance.- The intended application for this device requires that the frequency shall remain within the tolerance listed below under any combination of environment and input voltage conditions contained herein and over the specified period following initial calibration.

<u>TCVCXO Type</u>	<u>Overall Frequency Tolerance</u>	<u>Period</u>
TCVCXO-1	+10 ppm	2 weeks
TCVCXO-2	+10 ppm	1 year
TCVCXO-3	+30 ppm	1 year "

- \* Fig 2, delete present Fig 2 (used in Amd 3) and substitute revised Fig 2, "REMBASS TCVCXO SCHEMATIC"

Page 9

- \* Fig 3, delete in its entirety

Page 10

- \* Fig 4, delete in its entirety

NOTE: The margins of this amendment are marked with an asterisk to indicate where changes (additions, modifications, corrections, deletions) from the previous amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous amendment.





**APPENDIX B**  
**ELECTRONICS COMMAND**  
**TECHNICAL REQUIREMENTS**  
**SCS-512**

SHOCK RESISTANT CRYSTAL UNITS

1. SCOPE

1.1 Scope.- This specification covers the requirements and processing technique for shock resistant 20 MHz fundamental mode quartz crystal units.

2. APPLICABLE DOCUMENTS

2.1 Documents.- The following documents of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-C-3098	Crystal Units, Quartz.
MIL-H-10056	Holders, Crystal Standards.

OTHER

ECOM TR#4134	ECOM Technical Report: Packaging Precision Quartz Crystal Resonators.
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STANDARDS

FEDERAL

FED-STD-209	Clean Room and Work Station Requirements, Controlled Environment.
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MILITARY

MIL-STD-202	Test Methods for Electronic and Electrical Component Parts.
MIL-STD-883	Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both title and number or symbol should be stipulated when requesting copies.)

### 3. REQUIREMENTS

**3.1 General description.-** This specification covers the requirements for producing precision, shock resistant, microcircuit compatible, fundamental mode crystal units, in accordance with MIL-C-3098 and this document, over an operating temperature range of -40°C to 75°C.

**3.2 Performance characteristics.-** Performance characteristics of the crystal units apply over the full ambient operating temperature range of -40°C to 75°C (unless otherwise specified) and consist of Tables II and III, and as follows:

**3.2.1 Frequencies.-** The frequencies, at a load capacitance of 20 pF, shall be:

- (a) 17,000,000 Hz  $\pm$  170 Hz.
- (b) 19,200,000 Hz  $\pm$  192 Hz.
- (c) 20,000,000 Hz  $\pm$  200 Hz.
- (d) 22,000,000 Hz  $\pm$  220 Hz.

**3.2.2 Crystal resistance.-** The resonance resistance of the crystal units shall not exceed 6 ohms.

**3.2.3 Power level.-** 150 microwatts  $\pm$  10%.

**3.2.4 Capacitance.-** The unit's motional capacitance ( $C_1$ ) shall be 12.5 femto-farads  $\pm$  1.2 femto-farads. (See 4.7.7).

**3.2.5 Reliability - Crystal Units.-** The failure rate of crystal units shall not exceed 1%/1000 hours at a 60% confidence level when subjected to the test specified in 4.9.

**3.3 Design, construction, and physical dimensions.-** The crystal resonators shall be hermetically sealed in microcircuit compatible ceramic crystal enclosures HC-(XM-48)/U which are microcircuit equivalent to HC-18. The enclosure consists of a frame with a top and bottom lid as shown in Figure 2. Clips, such as the ones shown in Figure 3, are attached to the corners of the frame. A more complete package description can be found in ECOM Technical Report entitled "Packaging Precision Quartz Crystal Resonators."

3.4 Solderability.— Solder terminals shall be solderable. (See 4.7.1).

3.5 Shock.— The frequency change shall not exceed  $5 \times 10^{-7}$  after being subjected to shock forces of 1000g. (See 4.7.2).

3.6 Vibration.— After being subjected to a vibration of 20g peak at a frequency of 10 to 2000 Hz, the maximum change in the resonant frequency shall not exceed  $5 \times 10^{-7}$  and the maximum change in resonant resistance shall not exceed 10%. (See 4.7.3).

3.7 Reduced drive level.— When tested as specified in 4.7.8, the resistance shall not exceed 6 ohms.

3.8 Frequency and equivalent resistance.— The frequency and equivalent resistance of the crystal unit shall be within the limits specified in 3.2.1 and 3.2.2 respectively. (See 4.7.9).

3.9 Low-temperature storage.— When subjected to a temperature of  $-55^{\circ}\text{C}$  for 2 hours, the resistance shall be as specified in 3.2.2. (See 4.7.10).

3.10 Temperature run.— The frequency temperature characteristics shall be free of coupled modes, the frequency difference between the upper and lower turning points at resonance shall be  $18 \text{ ppm} \pm 3 \text{ ppm}$  and the resonance resistance shall not exceed 6 ohms. The maximum rate of change of resonance resistance with temperature shall not exceed  $0.2 \text{ ohms}/10^{\circ}\text{C}$  at any temperature in the range of  $-40^{\circ}\text{C}$  to  $75^{\circ}\text{C}$ . (See 4.7.11).

3.11 Thermal frequency repeatability.— The absolute values of the frequency changes  $f_{U1} - f_{U2}$ ,  $f_{U1} - f_{U3}$ ,  $f_{U2} - f_{U3}$ , and  $f_{L1} - f_{L2}$ , shall not exceed  $5 \times 10^{-8}$  when the crystal units are exposed to the prescribed temperature cycle. (See 4.7.6).

3.12 Unwanted modes.— There shall be no unwanted modes of oscillation (resonant frequencies other than the desired operating frequency) within  $\pm 20\%$  of the desired operating frequency. In addition, there shall be no abrupt frequency shifts and no intermittent oscillations. (Some crystal units may not start oscillating immediately at the plus 20 percent setting, or may cease oscillating during detuning, without resumption of oscillation on further detuning. These conditions are permitted.) (See 4.7.12).

3.13 Thermal shock.— When subjected to rapid changes in temperature between  $0^{\circ}\text{C}$  and  $100^{\circ}\text{C}$ , no part of the crystal unit shall crack, chip or break. (See 4.7.4).

3.14 Seal.- The leakage rate of the crystal units shall not exceed  $10^{-10}$  atm cc/sec. (See 4.7.5).

3.15 Salt spray (corrosion).- When subjected to a salt spray atmosphere there shall be no evidence of excessive corrosion. Corrosion that causes impairment of the electrical or mechanical performance of the unit shall be considered excessive. (See 4.7.13).

3.16 Moisture resistance.- After subjection of temperatures up to  $65^{\circ}\text{C}$  and a relative humidity of up to 100% for 10 days, the frequency and resistance of the crystal units shall be within the limits specified in 3.2.1 and 3.2.2, and the insulation resistance shall be not less than 500 megohms. (See 4.7.14).

3.17 Aging.- After 4 weeks stabilization at the upper turnover temperature and an additional 30 days at that temperature, at no time during the 30 days shall the crystal frequency deviate more than  $1 \times 10^{-8}$ /week. (See 4.7.15).

3.18 Accelerated aging.- After being conditioned in an oven at  $105^{\circ} \pm 3^{\circ}\text{C}$  for 168 hours and then allowed to stabilize at room ambient temperature, the difference in frequency between the measurements made immediately prior to and immediately after conditioning shall not exceed 0.5 ppm. After conditioning, the resonance resistance shall not exceed 6 ohms. (See 4.7.16).

3.19 Marking.- Marking shall be in accordance with MIL-C-3098.

3.20 Crystal processing requirements.-

3.20.1 Crystal processing flow chart.- Figure 1 is a flow chart of the minimum required manufacturing processes.

3.20.2 Resonator blank inspection.- When the resonator blanks are subjected to intense light at 10 X magnification there shall be no visible imperfections such as chips, cracks or scratches. (See 4.8.1).

3.20.3 Cleaning stations.- Crystal unit components exposed to the atmosphere shall be cleaned immediately prior to insertion into a vacuum chamber. The cleaning procedure shall result in surfaces which are free, on an atomic level, of both organic and inorganic contaminants.

3.20.3.1 Hydrophobic (organic) contamination.- The resonators shall be considered clean from hydrophobic (organic) contamination if uniform interference fringes are observed when they are subjected to condensation of water. (See 4.8.2.1).

3.20.3.2 Inorganic contamination.-- The crystal unit components shall be considered clean from inorganic contaminants if the resistivity of the final rinse water remains above  $10^{11}$  ohm-cm. (See 4.8.2.2).

3.20.4 Enclosure vacuum bakeout.-- Enclosure vacuum bakeout shall be performed at  $200^{\circ}\text{C} \pm 10^{\circ}\text{C}$  and  $10^{-7}$  torr pressure, minimum. (See 4.8.3).

3.20.5 Resonator vacuum bakeout.-- The resonators shall be baked in an oil free high vacuum system at a less than  $10^{-8}$  torr pressure. The bakeout temperature shall be variable up to  $400^{\circ}\text{C}$ . The resonators shall be free of hydrophobic contamination (see 3.20.3.1). (See 4.8.4).

3.20.6 Spot plating.-- Spot plating shall be performed in an oil free high vacuum system at less than  $10^{-7}$  torr pressure. The rate of deposition shall be variable, and the film thickness shall be monitored. Materials that have a strong adhesion to quartz, such as chromium-gold, shall be used. After the spot is subjected to a scratch by a metal instrument, there shall be no evidence of peeling at 100 X magnification. (See 4.8.5).

3.20.7 Resonator mounting and bonding.-- The resonators shall be mounted and bonded to the enclosure in a clean area, containing as a minimum, a laminar flow clean bench producing a cleanliness equivalent to Class 100 as defined in FED-STD-209 "Clean Room and Work Station Requirements, Controlled Environment." The bond shall be a nickel electrobond with a strength of at least 10 ounces. At the completion of the mounting and bonding process, the resonators shall cause no distortion in the reflection of a straight line from the resonator surface. The resonators shall then be inspected and cleaned as specified in 3.20.2 and 3.20.9. (See 4.8.6).

3.20.8 Final assembly.-- The last four processing operations; cleaning, bakeout, plating, and sealing, shall be performed without exposure of the vacuum systems and crystal unit components to contaminating atmosphere between operations. The high vacuum chambers shall have a base pressure of  $10^{-8}$  torr minimum. Only oil free pumps shall be used. All back-filling shall be with pure dry gases or controlled gas mixtures. Appropriate steps shall be taken to prevent dirt, loose particles and other forms of contaminants from being present in any of the chambers. The vacuum chambers shall be bakeable to  $250^{\circ}\text{C}$ . Provisions shall be made for flooding the entire inside of each processing chamber with short wave ultraviolet (UV) radiation in the presence of a partial pressure of oxygen. (See 4.8.7).

3.20.8.1 Cleaning.-- The mounted crystal resonators and package parts shall be cleaned immediately prior to the high vacuum operations for bake, plate and seal by short wave UV irradiation while in a partial pressure of oxygen. The length of time the crystal components are subjected to the UV irradiation, the wavelength of the UV irradiation, and the partial pressure of oxygen, shall be sufficient to produce the necessary concentration of ozone for cleaning. The resonators shall be considered clean from hydrophobic (organic) contamination if uniform interference fringes are observed when they are subjected to condensation of water. (See 4.8.7.1).

3.20.8.2 Bakeout.-- The mounted crystal units and package covers shall be vacuum baked prior to plating. The bakeout temperature shall be variable up to 450°C with a tolerance of  $\pm 5^\circ\text{C}$ . The vacuum during bakeout shall be  $10^{-6}$  torr minimum. (See 4.8.7.2).

3.20.8.3 Plating.-- The electrodes shall be deposited by thermal evaporation. In order to minimize stresses that could cause aging, the two sides of the resonator shall be plated simultaneously at equal rates, such that the final thicknesses of the electrodes shall be within 10% of one another. In order to minimize the aging due to mass transfer inside the completed resonator, the electrode material shall be of high purity, and it shall be deposited onto the crystal units rapidly so as to minimize the sorption of contaminants by the electrodes during deposition. The changing and outgassing of the evaporation sources and the replenishing and outgassing of the electrode material shall be performed in a "loading and outgassing" chamber. The pressure during plating shall not rise above  $1 \times 10^{-6}$  torr. The rate of evaporation shall be adjustable. The alignment of the electrodes shall be within 0.010 inch of the center of the crystal blanks and within 0.002 inch with respect to each other. Provisions shall be made for heating the mounted quartz blank during plating. Also, during plating, the crystal unit frequencies shall be monitored by means of a hermetically sealed oscillator located near the crystal unit's terminals. The temperature to which the blanks are heated during plating shall be variable up to 300°C with a tolerance of  $\pm 5^\circ\text{C}$ . (See 4.8.7.3).

3.20.8.4 Sealing.-- The sealing apparatus shall be capable of applying a force that is variable up to 1 ton, it shall be capable of heating the package up to 400°C with a tolerance of  $\pm 5^\circ\text{C}$ , and it shall be capable of providing combinations of these pressures and temperatures simultaneously. Gauges shall be provided with resolution appropriate for thermocompression bonding and for cold weld sealing. The sealed crystal units shall be transferred to the "unload" chamber for unloading so that the sealing chamber can remain under high vacuum continuously. Provision shall be made for sealing the crystal units in an inert atmosphere. (See 4.8.7.4).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection.-- Unless otherwise specified in the contract, the contractor is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

**4.2 Classification of inspection.**- Inspection shall be classified as follows:

- (a) Processing control inspection. (See 4.4).
- (b) First article inspection (does not include preparation for delivery). (See 4.5).
- (c) Quality conformance inspection. (See 4.6).

**4.3 Test plan.**- The contractor prepared Government-approved test plan, as cited in the contract, shall contain:

- (a) Time schedule and sequence of examinations and tests.
- (b) A description of the method of test and procedures.
- (c) Programs of any automatic tests including flow charts and block diagrams.
- (d) Identification and brief description of each inspection instrument with date of most recent calibration.

**4.4 Processing control inspection.**- Processing control shall consist of Table I in the order shown and all the tests included in the Government-approved test plan.

**4.5 First article.**- Unless otherwise specified in the contract, the first article inspection shall be performed by the contractor.

**4.5.1 First article units.**- The contractor shall furnish the number of crystal units at each frequency as specified in the contract. (See 3.2.1).

**4.5.2 First article inspection.**- The first article inspection shall consist of Tables I and II and all the tests included in the Government-approved test plan (See 4.3), to show compliance with the requirements of Section 3. No failures shall be permitted in Table II. The tests in Tables I and II are to be performed in the order shown.

**4.6 Quality conformance inspection.**- Quality conformance inspection shall consist of tests specified in Tables I, III, IV and paragraph 4.6.3 in the order shown.

**4.6.1 Group A inspection.**- Group A inspection shall consist of Table III. The inspection shall be made either on the same sample or separate samples for subgroups 1 and 2.



4.6.1.1 Sampling plan.- Statistical sampling and inspection shall be in accordance with MIL-STD-105 for general inspection level II. The acceptable quality level (AQL) shall be as specified in Table II. Major and minor defects shall be defined in Table V of MIL-C-3098 and MIL-STD-105.

4.6.2 Group B inspection.- Group B inspection shall consist of Table IV.

4.6.2.1 Sampling plan.- Statistical sampling and inspection shall be in accordance with MIL-STD-105 for special inspection level S-4. Major and minor defects are as defined in Table VI of MIL-C-3098 and MIL-STD-105.

4.6.3 Reliability.- Reliability test shall be as specified in 4.9.

4.7 Methods of examination and test.- Methods of examination and test shall be as specified in the appropriate tables and as follows:

4.7.1 Solderability.- Each terminal area shall be subjected to method 2002 of MIL-STD-883. (See 3.4).

4.7.2 Shock.- The crystal units shall be tested in accordance with MIL-STD-202, method 213B, Test Condition E, (except that the duration time shall be 6m sec) and one blow in each of three mutually perpendicular planes. The frequency shall then be measured in accordance with 4.7.9. (See 3.5).

4.7.3 Vibration.- The crystal units shall be tested for vibration per MIL-STD-202, method 204C, Test Condition D. The frequency and resonance resistance shall then be measured in accordance with 4.7.9. (See 3.6).

4.7.4 Thermal shock.- The crystal units shall be tested for thermal shock per paragraph 4.8.12.2 of MIL-C-3098. After completion of the test the units shall be examined for cracks, chips, or breaks. (See 3.13).

4.7.5 Seal.- The sealed crystal units shall be tested for hermeticity according to MIL-STD-202, method 112, Test Condition C, Procedure III. Back-fill pressure and gross leak test conditions used shall be as specified in the Government-approved test plan.

4.7.6 Thermal frequency repeatability.- The crystal units shall be subjected to the following temperature cycle:

(a) Heat from room temperature to the upper turning point temperature and, after thermal equilibrium is reached, measure the frequency ( $f_{U1}$ ) in accordance with 4.7.9.

(b) Heat to 85°C and maintain at this temperature for one hour.

(c) Lower the temperature to the upper turning point temperature and, after thermal equilibrium is reached, measure the frequency ( $f_{U2}$ ) in accordance with 4.7.9.

(d) Lower the temperature to the lower turning point temperature and, after thermal equilibrium is reached, measure the frequency ( $f_{L1}$ ) in accordance with 4.7.9.

(e) Cool the unit to  $-55^{\circ}\text{C}$  and maintain at this temperature for one hour.

(f) Raise the temperature to the lower turning point temperature and, after thermal equilibrium is reached, measure the frequency ( $f_{L2}$ ) in accordance with 4.7.9.

(g) Heat to the upper turning point temperature and, after thermal equilibrium is reached, measure the frequency ( $f_{U3}$ ) in accordance with 4.7.9.

**4.7.7 Capacitance.**— The unit's motional capacitance shall be measured by using an applicable crystal impedance meter specified in MIL-C-3098. (See 3.2.4).

**4.7.8 Reduced drive level.**— Reduced drive level shall be measured in accordance with paragraph 4.8.6 of MIL-C-3098. (See 3.7).

**4.7.9 Frequency and resonance resistance.**— Frequency and resonance resistance shall be measured in accordance with paragraph 4.8.8 of MIL-C-3098.

**4.7.10 Low-temperature storage.**— Crystal units shall be subjected to a temperature of  $-55^{\circ}\text{C}$  for 2 hours and shall then be measured for resistance with the crystal at a temperature of  $-55^{\circ}\text{C}$ . The resistance shall be measured at reduced drive level. (See 4.7.8 and 3.9).

**4.7.11 Temperature run.**— Temperature run shall be performed in accordance with paragraphs 4.8.10 and 4.8.10.1 of MIL-C-3098. (See 3.10).

**4.7.12 Unwanted modes.**— Unwanted modes shall be measured in accordance with paragraph 4.8.11.1 of MIL-C-3098. (See 3.12).

**4.7.13 Salt spray.**— Salt spray shall be performed in accordance with paragraph 4.8.14 of MIL-C-3098. The units shall then be inspected for excessive corrosion. (See 3.15).

Table I.- Process control requirements

Requirement	Reqt Para	Test Para	No. units tested per each batch <sup>1/</sup>	Frequency of test	Failure Evaluation
Resonator blank inspection	3.20.2	4.8.1	All	each resonator	2/
Cleaning stations	3.20.3	4.8.2	1	each batch	3/
Enclosure vacuum bakeout	3.20.4	4.8.3	1	" "	3/
Resonator vacuum bakeout	3.20.5	4.8.4	1	" "	3/
Spot plating	3.20.6	4.8.5	1	" "	4/
Resonator mounting and bonding	3.20.7	4.8.6	As specified in 4.8.6	" "	As specified in 4.8.6
Cleaning stations	3.20.3	4.8.2	1	" "	3/
Resonator blank inspection	3.20.2	4.8.1	All	each resonator	2/
Final assembly:	3.20.8	4.8.7	As specified in 4.8.7	each batch	As specified in 4.8.7
Cleaning	3.20.8.1	4.8.7.1			
Bakeout	3.20.8.2	4.8.7.2			
Plating	3.20.8.3	4.8.7.3			
Sealing	3.20.8.4	4.8.7.4			

<sup>1/</sup> A batch shall be defined as a group of crystal unit components which are subjected to a specific process at one time.

<sup>2/</sup> Failed units shall be rejected.

<sup>3/</sup> A failure shall require batch be rejected or recycled.

<sup>4/</sup> A failure shall require batch be rejected.

Table II.- First article

Examination or test	Reqd Para	Method Para	No. Units to be tested <sup>1/</sup>
Visual and mechanical examination (external)	3.2, 3.3	4.7.17	15
Solderability	3.4	4.7.1	15
Shock	3.5	4.7.2	15
Vibration	3.6	4.7.3	15
Reduced drive level	3.7	4.7.8	15
Capacitance	3.2.4	4.7.7	15
Frequency and equivalent resistance	3.8	4.7.9	15
Low-temperature storage	3.9	4.7.10	15
Temperature run	3.10	4.7.11	15
Thermal frequency repeatability	3.11	4.7.6	15
Unwanted modes	3.12	4.7.12	15
Thermal shock	3.13	4.7.4	15
Seal	3.14	4.7.5	15
Salt spray (corrosion)	3.15	4.7.13	3
Moisture resistance	3.16	4.7.14	3
Aging	3.17	4.7.15	15
Visual and mechanical examination (internal)	3.2, 3.20.6, 3.20.7, 3.20.8.3	4.7.17	2
Reliability <sup>2/</sup>	3.2.5	4.9	46

<sup>1/</sup>This is the number of units at each frequency to be tested (see 3.2.1), except for Reliability test.

<sup>2/</sup>The lot of 46 units selected must be representative of the four frequencies.

Table III.- Group A inspection

Examination or test	Reqd Para	Method Para	AQL (percent defective)	
			Major	Minor
<u>Subgroup 1</u>				
Visual and mechanical examination (external) 1/	3.2,3.3	4.7.17	-	-
Shock	3.5	4.7.2	1.0	-
Reduced drive level	3.7	4.7.8		
Frequency and resonance resistance	3.8	4.7.9		
Low-temperature storage	3.9	4.7.10		
Temperature run	3.10	4.7.11		
Thermal frequency repeatability	3.11	4.7.6		
Unwanted modes	3.12	4.7.12		
Seal	3.14	4.7.5		
<u>Subgroup 2</u>				
Accelerated aging	3.18	4.7.16	1.0	-

<sup>1/</sup>Two sample units only for external dimensions. No failures permitted.

Table IV.- Group B inspection

Examination or test	Reqt Para	Method Para.	AQL (percent defective)	
			Major	Minor
Solderability	3.4	4.7.1	1.0	-
Capacitance	3.2.4	4.7.7		
Shock	3.5	4.7.2		
Vibration	3.6	4.7.3		
Thermal shock	3.13	4.7.4		
Seal	3.14	4.7.5		
Salt spray (corrosion)	3.15	4.7.13		
Moisture resistance	3.16	4.7.14		
Visual and mechanical examination (internal)	3.2, 3.20.6, 3.20.7, 3.20.8, 3	4.7.17		

4.7.14 Moisture resistance.- Moisture resistance shall be performed in accordance with paragraph 4.8.15 of MIL-C-3098. Frequency and resonance resistance shall then be measured in accordance with 4.7.9. (See 3.16).

4.7.15 Aging.- Aging shall be performed in accordance with paragraph 4.8.16 of MIL-C-3098. (See 3.17).

4.7.16 Accelerated aging.- Accelerated aging shall be performed in accordance with paragraph 4.8.16.1 of MIL-C-3098. (See 3.18).

4.7.17 Visual and mechanical examination.- Visual and mechanical examination shall be performed in accordance with paragraph 4.8.2 of MIL-C-3098.

4.8 Processing control inspections.- The following inspections are performed as specified during the fabrication of the crystal units.

4.8.1 Resonator blank inspection.- Each resonator blank shall be inspected for chips, cracks and scratches under intense light at 10 X magnification. Only those crystal blanks which are free of visible imperfections at 10 X magnification shall be processed. This inspection shall also be performed prior to final assembly. (See 3.20.2 and 3.20.7).

4.8.2 Cleaning stations.-

4.8.2.1 Hydrophobic (organic) contamination.- The resonators shall be checked for hydrophobic contamination by selecting one wafer from each batch and holding it over hot distilled and deionized water so as to produce condensation. The resulting interference fringes are then observed over the whole surface facing the water for uniformness. (See 3.20.3.1).

4.8.2.2 Inorganic contamination.- The resonators shall be checked for inorganic contaminants prior to insertion into the final processing system by monitoring the resistivity of the final rinse water. (See 3.20.3.2).

4.8.3 Enclosure vacuum bakeout.- Suitable measuring devices shall be used to record a temperature of  $800^{\circ}\text{C} \pm 10^{\circ}\text{C}$  and a pressure of less than  $10^{-7}$  torr in the vacuum bakeout oven. (See 3.20.4).

4.8.4 Resonator vacuum bakeout.- One resonator from each batch shall be held over hot distilled and deionized water so as to produce condensation. The interference fringes on the whole surface facing the water shall be observed for uniformness. (See 3.20.5).

**4.8.5 Spot plating.-** The spots shall be scratched with a sharply pointed metal instrument (such as a straight pin) and then observed at 100 X magnification. Units subjected to this test shall not be delivered on the contract. (See 3.20.6).

**4.8.6 Resonator mounting and bonding.-** After mounting and bonding, each unit shall be inspected for distortion by observing the reflection of a straight line from the resonator surface. The strength of the electrobond shall be determined by performing a pull test on one unit from end batch processed. Units subjected to the pull test shall not be delivered on the contract. (See 3.20.7).

**4.8.7 Final assembly.-** At the completion of the final four processes, (cleaning, bakeout, plating and sealing), each batch shall contain a unit that has not been sealed. This unit shall then be examined for cleanliness (see 4.8.7.1) and plating (see 4.8.7.3). (See 3.20.8). If unit fails cleanliness and/or plating requirements, the entire batch shall be rejected.

**4.8.7.1 Cleaning.-** The resonators shall be inspected for hydrophobic contamination using the method described in 4.8.3.1. (See 3.20.8.1).

**4.8.7.2 Bakeout.-** Suitable measuring devices shall be used to ascertain the actual temperature (and accuracy to which it is maintained), and pressure of the vacuum bakeout oven.

**4.8.7.3 Plating.-** A visual and mechanical examination in accordance with paragraph 4.8.2 of MIL-C-3098 will be made to insure the alignment of the electrodes conforms to 3.20.8.3. Suitable measuring devices shall be used to monitor the plating chamber pressure and the resonator temperature. (See 3.20.8.3).

**4.8.7.4 Sealing.-** A seal test will be performed on one unit from each batch using the method described in 4.7.5. Suitable measuring devices shall be used to record sealing force and temperature during the sealing process. (See 3.20.8.4).

#### **4.9 Reliability.-**

**4.9.1 Prerequisite.-** The crystal units to be used for this evaluation shall be selected from lots which have successfully completed Groups A and B inspections. (See 3.2.5).

**4.9.2 Reliability test oven.-** The units selected for the reliability evaluation shall be stored in an oven maintained at the upper turnover temperature and stable to at least  $\pm 0.01^\circ\text{C}$ . The oven shall be constructed with suitable electrical connectors so each crystal unit can be oscillated and measured to the required accuracy.



**4.9.3 Reliability test cycle.**-- The reliability test cycle shall consist of submitting 50 units of each frequency (200 units total) to the following sequence of tests which shall be repeated at weekly intervals. All frequency measurements shall be made in a measurement system capable of measurements reproducible to 2 parts in  $10^9$ :

(a) Resonance resistance measurements shall be made in the test set prior to inserting the crystals in the oven and after removal from the oven on completion of the test.

(b) After insertion in the oven the crystal units shall be stabilized for 4 weeks at the upper turnover point prior to beginning the reliability test cycle.

(c) Measure and record the resonant frequency of each crystal unit 4 weeks after the oven stabilizes at the upper turnover point.

(d) The crystal units shall be maintained at the upper turnover point for an additional 6 weeks. Measure and record the resonant frequency of each crystal unit during this period.

**4.9.4 Reliability evaluation.**-- The test data obtained from the twice weekly measurements during the test cycle shall be evaluated at the end of the 6 week period. Units showing a frequency change of more than  $1 \times 10^{-8}$  per week during the test period shall be classified as failures.

**4.9.5 Failure-rate criteria.**-- When subjected to the reliability test cycle specified above, the failure rate shall not exceed  $1\%/1000$  hours at a 60% confidence level (i.e. equivalent to 1 failure for 200 units over a 1000 hour period of testing).

## **5. PREPARATION FOR DELIVERY**

**5.1** Preparation for delivery shall be as specified in the contract.

## 6. NOTES

**6.1 Processing facility accommodations.**- The processing equipment should accommodate, as a minimum, the four different sizes of microcircuit compatible crystal enclosures as follows:

- (a) The microcircuit compatible equivalent of the HC-6.
- (b) The microcircuit compatible equivalent of the HC-18.
- (c) The microcircuit compatible equivalent of the HC-32.
- (d) The microcircuit compatible equivalent of the HC-44.

The term "equivalent" as used here means that the dimensions of the new enclosure will fit within the space described by the outside dimensions of the corresponding enclosures referred in MIL-H-10056. The inside dimensions of the new enclosures should be suitable for accommodating the range of resonator diameter normally accommodated in the respective enclosures of MIL-H-10056. The minimum diameter to thickness ratio of the resonator which the enclosure should be able to accommodate is thirty.

**6.2 Processing facility capability.**- The processing facility should be capable of the following:

- (a) Processing a minimum of 200 acceptable crystal units per 8 hour day with a minimum yield of 66%.
- (b) Full capacity operation, without breakdowns, for a minimum of five consecutive days. (A breakdown shall be defined as any equipment related occurrence that causes an interruption of the normal fabrication routine for more than 10 minutes per 8 hour work day.)
- (c) Final assembly (cleaning, bakeout, plating, and sealing) should be performed using as much automated equipment as economically feasible.

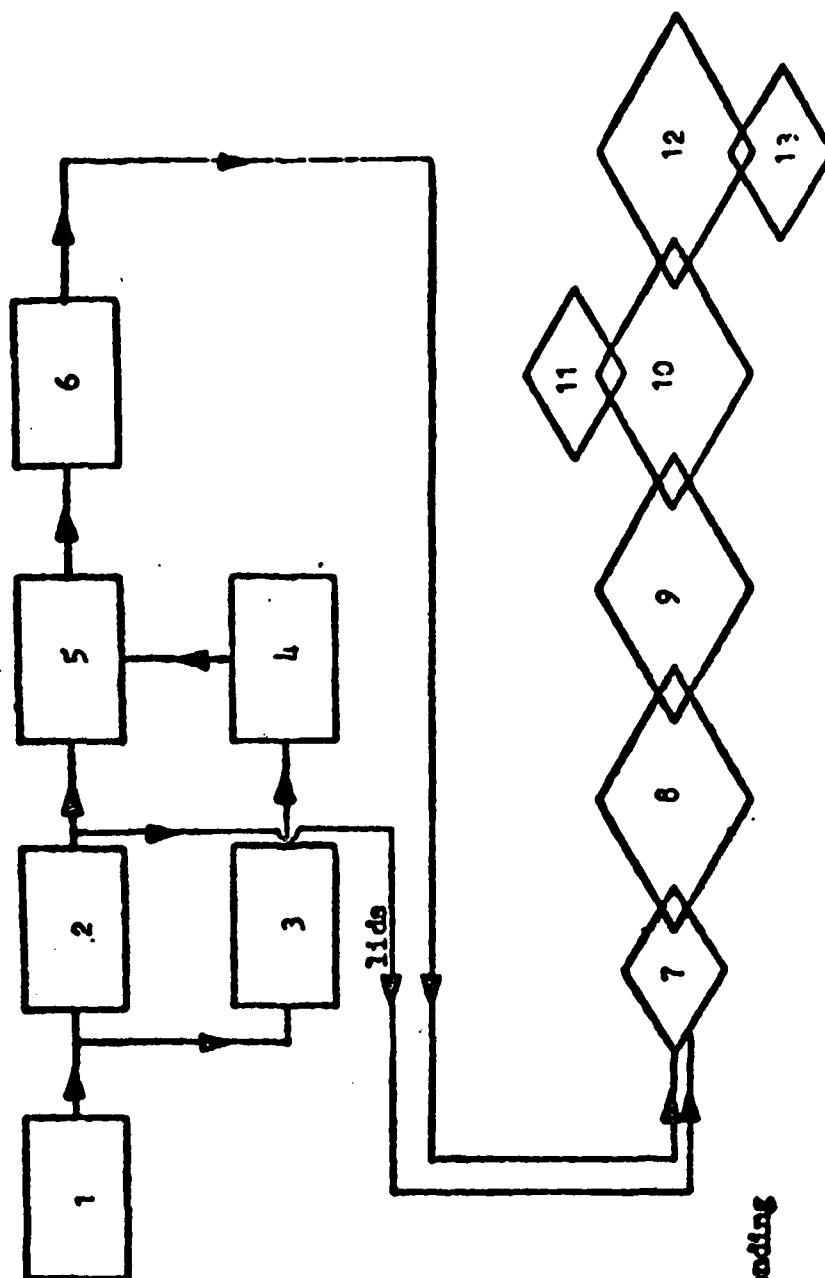
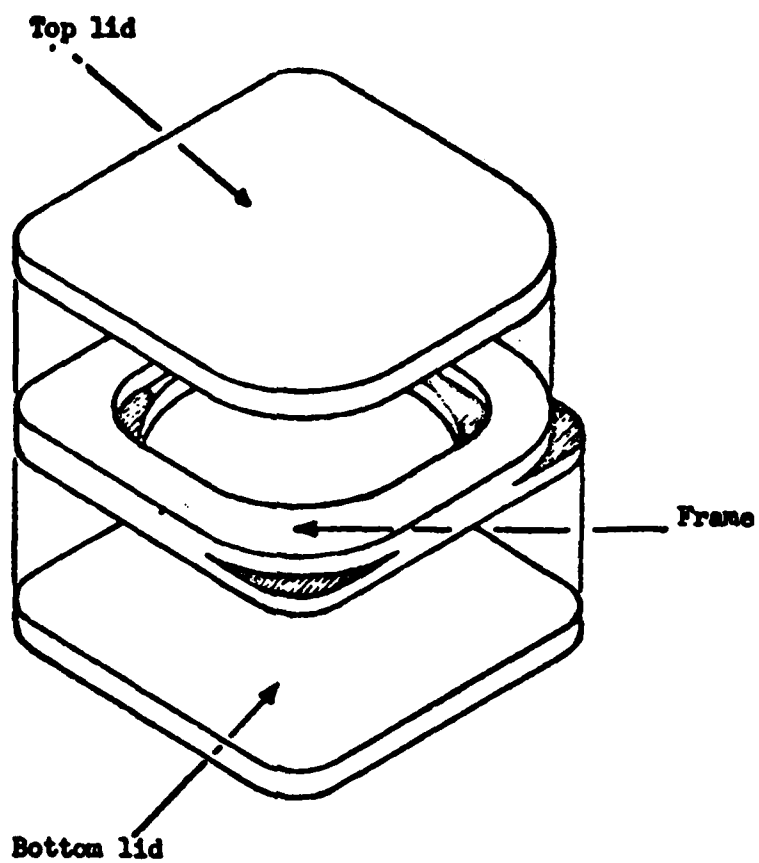


Figure 1. Crystal Processing Flow Chart

- 1 Clearing station  
 2 Vacuum furnace - enclosure  
 3 Vacuum furnace - resonator  
 4 Spot plating station  
 5 Clean area: mounting & bonding  
 6 Cleaning station  
 7 Loading chamber  
 8 Cleaning chamber  
 9 Bakeout chamber  
 10 Plating chamber  
 11 Loading & outgassing chamber (filaments)  
 12 Sealing chamber  
 13 Unloading chamber



**Figure 2A. EXPLODED VIEW OF THE QUARTZ RESONATOR PACKAGE.**

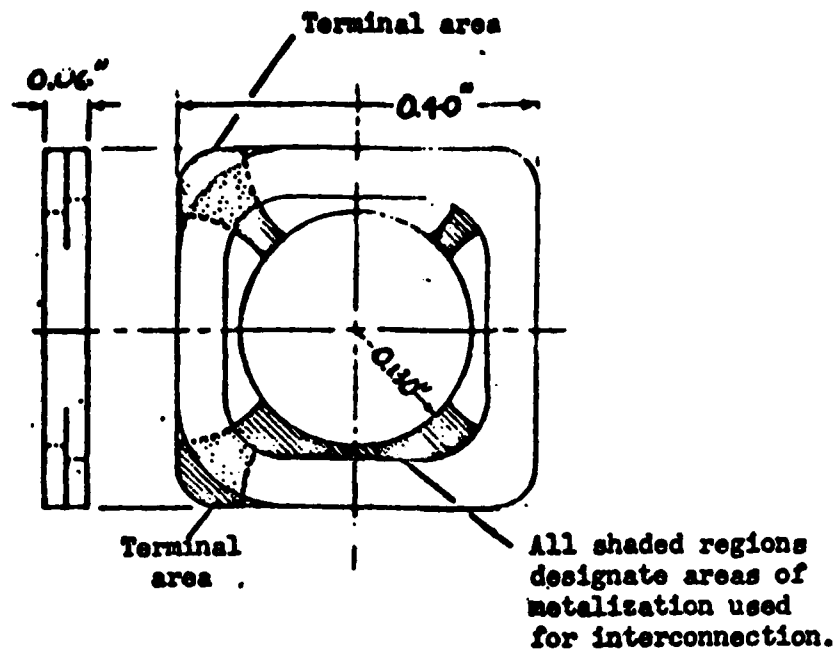


Figure 2B. FRAME FOR THE QUARTZ RESONATOR PACKAGE

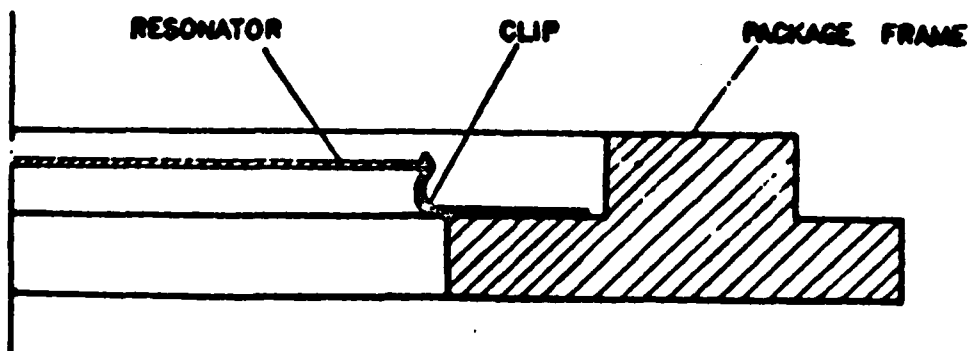
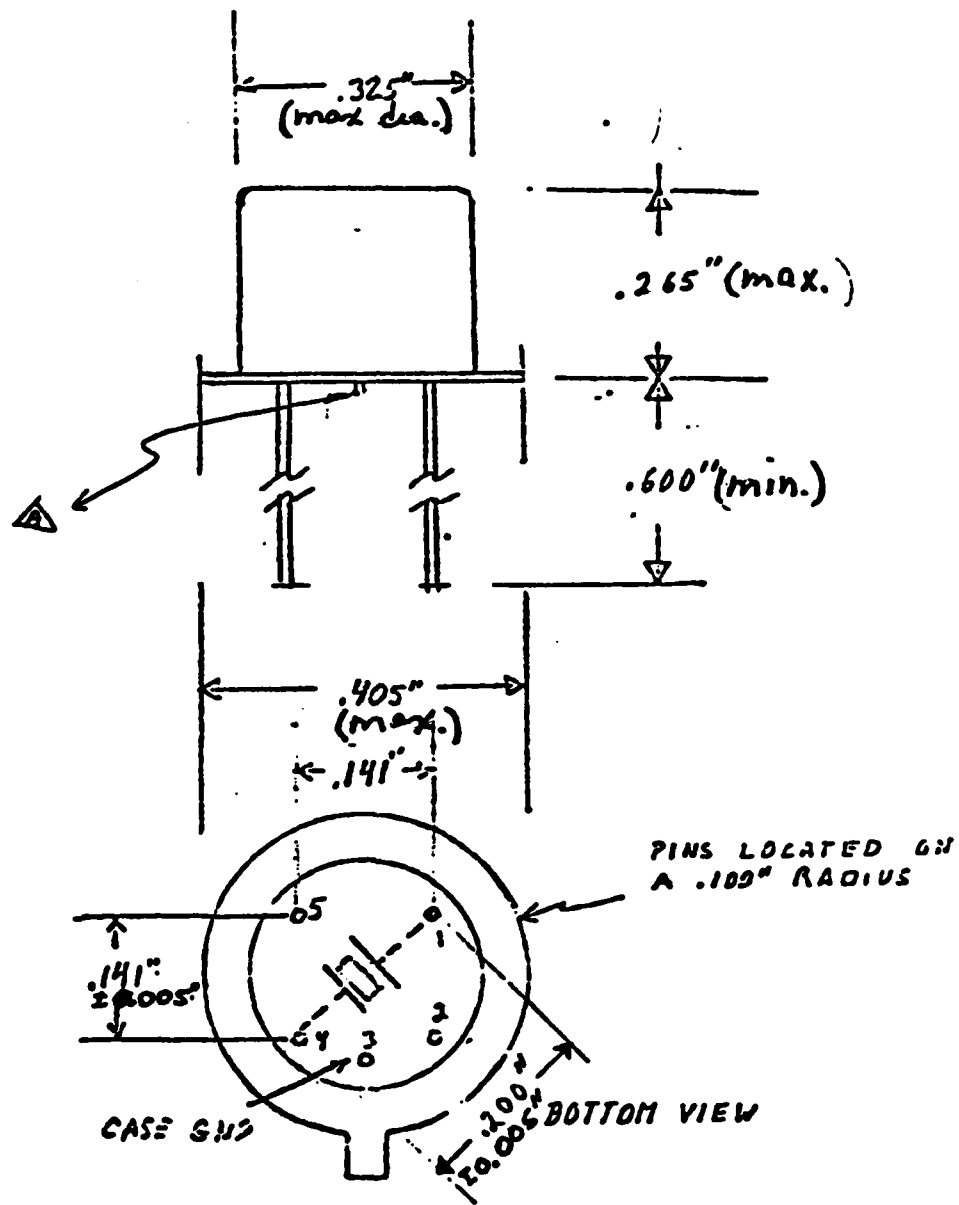


Figure 3. CROSS SECTION OF PACKAGE FRAME SHOWING RESONATOR AND MOUNTING CLIP CONFIGURATION

PIEZO CRYSTAL COMPANY  
CRYSTAL UNIT REMBASS-4



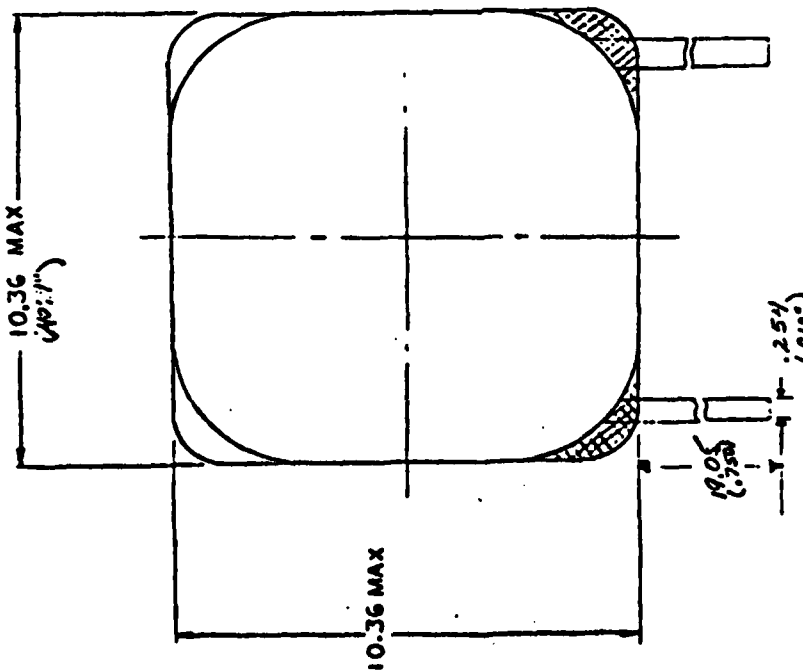
△ NOTE: PINS 2, 3, 5  
are clipped to  
within  $.0625''$  of  
bottom of base

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# SIMETRIC



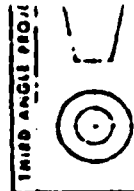
3.04 MAX  
(1.20")

2.54 MAX  
(0.10) inches

## NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN MILLIMETRES.
2. APPLIED PRACTICE PER ITEM 9.
3. PROCEDURE:
  - 3.1 ULTRAVIOLET CLEAN ITEM 2 & 3 PER ITEM 4, FOR 5 MIN MIN./5.
  - 3.2 VACUUM SEAL ITEM 4 TO ITEM 2 PER ITEM 5.

QTY	PT NO	DESC	ITEM
X		ASSEMBLY	1
1	45C923772G1	FRAME/RESON. EVAP.	2
2	468923756G2	COVER/GASKET ASH.	3
X	SS305131-200	U.V. CLEANING	4
X	468923770G1	SEALING	5
X	99000000	GEN. MFG. REQ	6



APPROVALS	DATE	INITIALS	REVISION
DESIGNED	10/6/75	ER	
CHECKED	10/6/75	ER	
PART CLASSIFICATION			
UNCLASSIFIED			
ONE CLASSIFICATION LEVEL			
UNCLASSIFIED			

CR-XM-159/U RESONATOR	
DATE	20/11/75
FOR	14064
ITEM NO.	46E9237
SCALE	1:1

GROUP 1018

PC-3

MIL-H-10056/9B  
1 March 1966  
SUPERSEDING  
MIL-H-10056/9A  
6 July 1965

## MILITARY SPECIFICATION

HOLDER, CRYSTAL, TYPE HC-18/U

This specification is mandatory for use by all  
Departments and Agencies of the Department of  
Defense.

### 1. SCOPE

1.1 This specification covers the detail requirements for type HC-18/U crystal holders.

Note: NATO Preferred type 3.

### 2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

#### SPECIFICATIONS

##### FEDERAL

QQ-C-585 - Copper-Nickel-Zinc-Alloy Plate, Sheet, Strip, and Bar (Copper Alloy Numbers 735, 745, 752, 762, 766, and 770).

##### MILITARY

MIL-H-10056 - Holders, Crystal, General Specification for.  
MIL-F-14072 - Finishes for Ground Signal Equipment.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

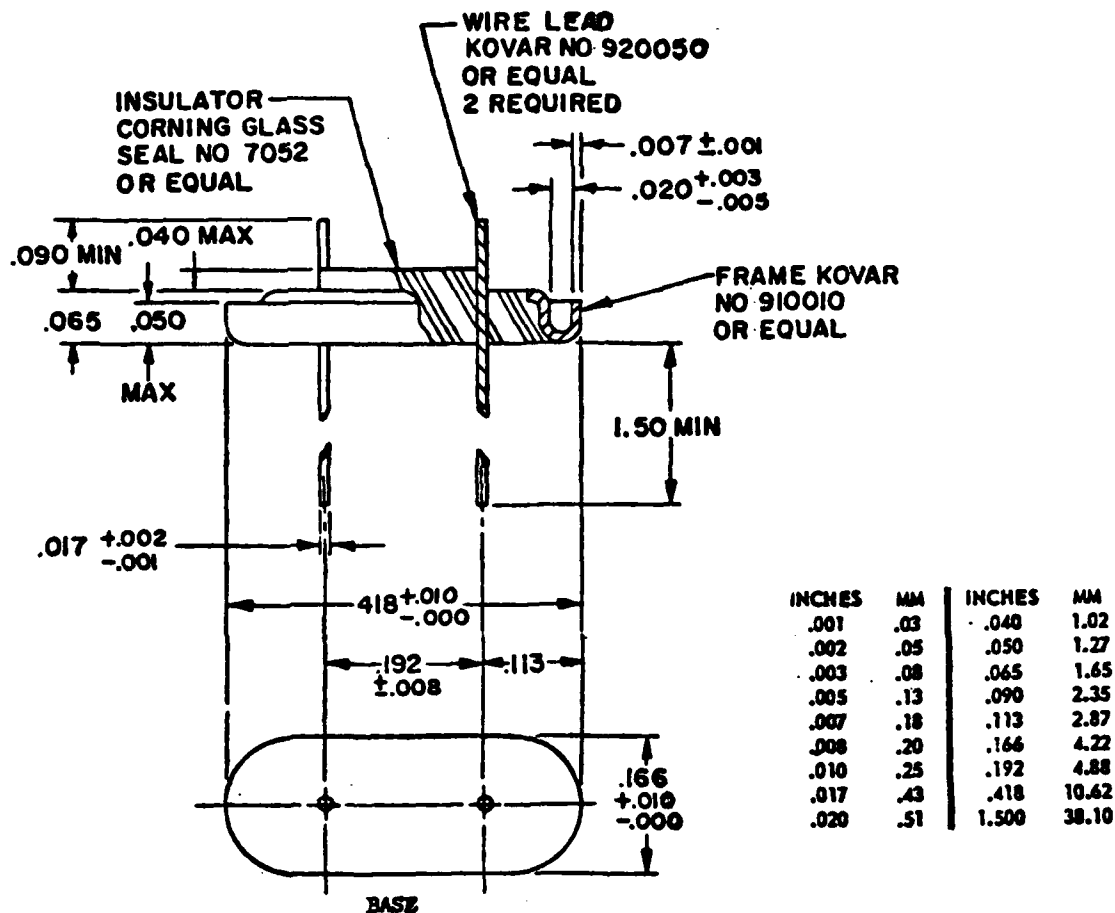
### 3. REQUIREMENTS

3.1 General. Requirements shall be in accordance with MIL-H-10056, and as specified herein.

3.2 Design and construction. Crystal holders shall be of the design, construction, and physical dimensions specified on figure 1.

FSC 5955





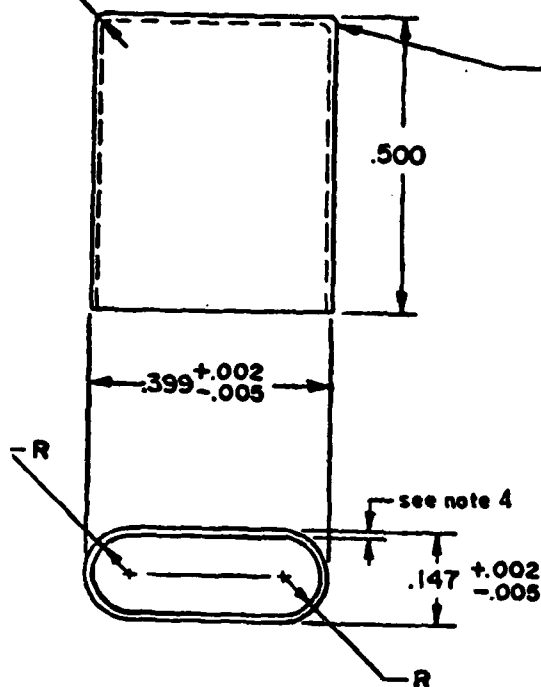
# NOTES:

1. After assembling, base assembly (lead and frame) shall be hot-tin-dipped or electro-tin-plated in accordance with type 1 finish of MIL-F-14072.
2. Unless otherwise specified, tolerance is  $\pm .005$  on decimals.
3. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
4. Before forming, the cover shall be  $.008 \pm .001$  inch thick or may be  $.010 \pm .001$  inch thick providing the inside edge is shaved to  $.008 \pm .001$  inch to a height of  $5/64$  (1.98 mm) inch above the open end.

FIGURE 1. Type HC-18/U crystal holder. (Continued)

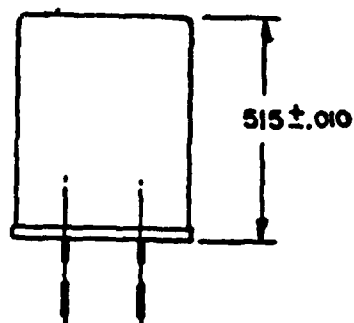
MIL-H-10056/9B

0.15 R



INCHES	MM
.002	.05
.005	.13
.010	.25
.015	.38
.126	3.20
.147	3.73
.392	9.96
.399	10.13
.500	12.70
.515	13.08

COVER  
PER QQ-C-585 COMPOSITION  
NO. 6 ANNEALED SOFT TEMPER



ASSEMBLY BEFORE SOLDERING

FIGURE 1. Type HC-18/U crystal holder.

MIL-H-10056/9B

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-H-10056.

#### 5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery shall be in accordance with MIL-H-10056.

#### 6. NOTES

6.1 The notes specified in MIL-H-10056 are applicable to this specification.

6.2 This crystal holder meets the design requirements in accordance with NATO Agreement STANAG 4032.

\* 6.3 The margins of this specification are marked with an asterisk to indicate where changes (additions, modifications, corrections, deletions) from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

#### Custodians:

Army - EL  
Navy - SH  
Air Force - 11

#### Preparing activity:

Army - EL

(Project 5955-0310-1)

#### Review activities:

Army - MI, MU, SM, EL  
Navy - SR  
Air Force - 11, 17, 85

#### User activities:

Army -  
Navy - WP, MC, CG  
Air Force - 14, 19

APPENDIX C  
TCVCXO NETWORK ADJUSTMENT  
AND RESISTOR TRIM PROCEDURE

21 December 1977

The VCXO Network Adjustment and Trim Procedure as submitted and approved in the First Quarterly Report and as subsequently amended is further amended as follows:

1. Paragraphs 2 - Digital Deviation - and 3 - Analog Center Frequency - are deleted in their entirety.
2. Paragraph 4 - Analog Deviation - Sub-paragraph entitled "Object", amend tolerance to read " $0.5\%$ " in lieu of " $\pm 5\%$ ".
3. Paragraph 4 - Analog Deviation - Sub-paragraph entitled "Conditions" is amended as follows:
  - A. Sub-sub-paragraph "b." is deleted in its entirety and replaced by "b." DVM (Ratiometer) across U5 input  $E_{ANLG}$  output (TPI) and ground."
  - B. Sub-sub-paragraph "d." delete " $3.5V$ " and replace by " $6.0V$ ".
  - C. Sub-sub-paragraphs "e" and "f" are deleted in their entirety.
4. Paragraph 4 - Analog Deviation - Sub-paragraph entitled "Trim Procedure" is amended as follows:

Delete everything beginning with "Inject  $1V \pm 0.02V$  RMS..." and ending with " $1V \pm 0.02V$  RMS at TPI" and replace with "Inject  $1KHz$  signal ( $1V$  RMS maximum) across  $E_{ANLG}$  interconnect and ground. Trim R63 to set gain (ratio) at  $1.0 \pm 0.5\%$ ".
5. Paragraph 5 - Compensation Gain - Sub-paragraph entitled "Object" - after "... voltage gain at U5 equals" add " $1.1 \pm 0.5\%$ " and delete the balance of the sub-paragraph.
6. Paragraph 5 - Compensation Gain - Sub-paragraph entitled "Conditions" is amended as follows:
  - A. Sub-sub-paragraph "b." - Delete in its entirety and replace with "DVM (ratiometer) across U5 input ( $E_{COMP}$ ) out (TPI) and ground."
  - B. Sub-sub-paragraph "d." - Delete in its entirety.
  - C. Sub-sub-paragraph "e." - Delete " $E_{DIG}$ ".
  - D. Sub-sub paragraph "f." - Delete in its entirety.
7. Paragraph 5 - Compensation Gain - Sub-paragraph entitled "Trim Procedure" is amended as follows:

Delete everything beginning with "Inject 1V + 0.02 V RMS..." and ending with "...Fx/Fs V  $\pm$  0.02 V RMS at TPI." and replace with "Inject 1 KHz signal (1V RMS maximum) across E<sub>COMP</sub> interconnect and ground. Rrim R64 to set gain (ratio) to 1.1  $\pm$  0.5%"

8. The following changes for Confirmatory and Pilot Run samples are instituted:

A. Drawing ES-B-212776

Sever metallization of pins 8 and 9 on VCXO tab adjacent to moat such as to divorce connector capacitance from crystal.

Reason: To permit either handwiring to the TCVCXO or plugging it into a connector without affecting performance.

B. Raytheon Drawing 32199

VCXO functional trim fixturing modification involving solder attachment of crystal to circuit in moat area.

Reason: To eliminate introduction of undesirable stray capacity across crystal and permit meshing of requirements.

C. Deletion of digital modulation and analog transmission control functions which involve:

(1) Drawing ES-C-215281

Exclusion of CMOS device U3 and U4 from circuit.

(2) Raytheon Drawing 31370 Rev A

Elimination of need for passive trimming resistors R61, R62, R65, R66, R69 and R70.

(3) VCXO Network Adjustment and Trim Procedure

Elimination of active trim steps 2 and 3 of the VCXO trim procedure.

(4) VCXO Network Adjustment and Trim Procedure

Minor modification of trim procedure.

(5) Drawing ES-C-215281

Passive trim of R105 to 23K.

Reason: Elimination of digital modulation function in REMBASS TCVCXO.

D. Drawing ES-C-215281

Jump (bridge) 9V and E<sub>DIG</sub> interconnects.

Reason: To provide regulated 9V output at pin 1.

Arthur Rothman  
Procuring Contracting  
Officer

## VCXO NETWORK ADJUSTMENT AND TRIM PROCEDURE

### 1. 9 V REGULATOR

OBJECT: Adjust regulator output to  $9.000 \text{ V} \pm 0.002 \text{ V}$

CONDITIONS: a. 12 V power supply across 12 V interconnect and ground.  
b. DVM across 9 V interconnect and ground.

TRIM PROCEDURE: If DVM  $< 8.998 \text{ V}$ , trim R98  
If DVM  $> 9.002 \text{ V}$ , trim R97

### 2. DIGITAL DEVIATION

OBJECT: Adjust U4 voltage level such that TPI difference voltage, corresponding to logic 0 and 1 inputs at the  $E_{DIG}$  interconnect equals  $1.250 \text{ V} \pm 0.002 \text{ V}$

CONDITIONS: a. 12 V power supply across 12 V interconnect and ground  
b. DVM across TPI interconnect and ground  
c.  $25 \text{ k}\Omega$  potentiometer across Fadj (Pin 6) and ground  
d. 3.5 V across  $E_{COMP}$  interconnect and ground  
e.  $E_{CNTRL} = E_{ANLG} = 0 \text{ V}$  (interconnects at ground potential).  
f.  $E_{DIG} = 5 \text{ V}$

TRIM PROCEDURE: Set TPI =  $4.000 \text{ V} \pm 0.001 \text{ V}$  using  $25 \text{ k}\Omega$  pot.  
Make  $E_{DIG} = 0 \text{ V}$  (ground potential).  
If DVM  $< 2.749$  trim R72  
If DVM  $> 2.751$  trim R71

### 3. ANALOG CENTER FREQUENCY

OBJECT: Adjust U3 voltage level such that TPI difference voltage, corresponding to logic 0 and 1 inputs at the  $E_{CNTRL}$  interconnect, equals  $0.625 \pm 0.002 \text{ V}$ .

CONDITIONS: a. 12 V power supply across 12 V interconnect and ground.  
b. DVM across TPI interconnect and ground.  
c.  $25 \text{ k}\Omega$  potentiometer across Fadj (Pin 6) and ground.  
d. 3.5 V across  $E_{COMP}$  interconnect and ground.  
e.  $E_{ANLG} = E_{DIG} = 0 \text{ V}$  (ground potential).  
f.  $E_{CNTRL} = 5 \text{ V}$

TRIM PROCEDURE: Set TPI =  $4.125 \text{ V} \pm 0.001$  using  $25 \text{ k}\Omega$  pot.  
Make  $E_{CNTRL} = 0 \text{ V}$  (ground potential).  
If DVM  $< 3.499 \text{ V}$ , trim R70  
If DVM  $> 3.501 \text{ V}$ , trim R69



#### 4. ANALOG DEVIATION

**OBJECT:** Adjust R63 summing resistor such that analog voltage gain at U5 equals  $T.0 \pm 5\%$ .

- CONDITIONS:**
- a. 12 V power supply across 12 V interconnect and ground.
  - b. DVM (AC/DC) across TPI interconnect and ground.
  - c. 25 k $\Omega$  potentiometer across Fadj (Pin 6) and ground.
  - d. 3.5 V across E<sub>COMP</sub> interconnect and ground.
  - e. E<sub>CNTRL</sub> = 5 V.
  - f. E<sub>ANLG</sub> = E<sub>DIG</sub> = 0 V (ground potential).

**TRIM PROCEDURE:** Set TPI = 3.5 V d.c. using 25 k $\Omega$  pot.  
Inject 1 V  $\pm 0.02$  V rms 1 kHz signal across E<sub>ANLG</sub> interconnect and ground.  
Trim R63 to get 1 V  $\pm 0.02$  V rms at TPI.

#### 5. COMPENSATION GAIN

**OBJECT:** Adjust R64 summing resistor such that temperature compensation voltage gain at U5 equals  $F_x/F_s$  volts, where  $F_x$  is the nominal frequency of the assigned crystal and  $F_s$  is the nominal frequency of the crystal from which the standard cubic correction function was derived.  $F_s = 20.50$  MHz for compensation DFG resistor values in TCVCX0 Schematic ES-C-215261.

- CONDITIONS:**
- a. 12 V power supply across 12 V interconnect and ground.
  - b. DVM (AC/DC) across TPI interconnect and ground.
  - c. 25 k $\Omega$  potentiometer across Fadj (Pin 6) and ground.
  - d. E<sub>CNTRL</sub> = 5 V.
  - e. E<sub>DIG</sub> = E<sub>ANLG</sub> = 0 V (ground potential)
  - f. E<sub>COMP</sub> = 3.5 V d.c.

**TRIM PROCEDURE:** Set TPI = 3.5 V d.c. using 25 k $\Omega$  pot.  
Inject 1 V  $\pm 0.02$  V rms 1 kHz signal at E<sub>COMP</sub> (audio generator in series with 3.5 V supply).  
Trim R64 to get  $\frac{F_x}{F_s}$  V  $\pm 0.02$  V rms at TPI.

#### 6. F/V LINEARIZATION

**OBJECT:** Adjust linearization DFG segment gains to linearize VCX0 frequency/voltage tuning characteristic for a slope of 500 Hz/V.

- CONDITIONS:**
- a. 12 V power supply across 12 V interconnect and ground.
  - b. 25 k $\Omega$  potentiometer across Fadj (Pin 6) and ground.
  - c. 1 k $\Omega$  load and frequency counter across RF (Pin 7) and ground.
  - d. Crystal connected across Pin 8 and 9.
  - e. DVM at E<sub>0</sub> (term. 6, U6) and at TPI

TRIM PROCEDURE:

Set TPI = 1.5 V  $\pm 0.001$  V using 25 k $\Omega$  pot.

If  $E_0 > 1.001$  Trim R76

If  $E_0 < 0.999$  Trim R104

At  $E_0 = 1.000$  V  $\pm 0.001$  V, record freq. ( $F_{REF}$ )

Set TPI = 3.5 V  $\pm 0.001$  V using 25 k $\Omega$  pot. Note frequency ( $F_1$ )

If ( $F_1 - F_{REF}$ )  $> 1002$  Hz, trim R78

If ( $F_1 - F_{REF}$ )  $< 998$  Hz, trim R75

( $F_1 - F_{REF}$ ) should equal 1000 Hz  $\pm 2$  Hz

Set TPI = 5.5 V  $\pm 0.001$  V using 25 k $\Omega$  pot. Note frequency ( $F_2$ )

If ( $F_2 - F_{REF}$ )  $> 2002$  Hz, trim R83

If ( $F_2 - F_{REF}$ )  $< 1998$  Hz, trim R80

( $F_2 - F_{REF}$ ) should equal 2000 Hz  $\pm 2$  Hz

## COMPENSATION NETWORK ADJUSTMENT AND TRIM PROCEDURE

### 1. THERMOMETER GAIN

**OBJECT:** Adjust R2 or R6 summing resistors such that the gain for the voltage across CRI equals  $8.5 \pm 5\%$ .

**CONDITIONS:**

- a. Regulated 9 V  $\pm 0.001$  V across 9V interconnect and ground.
- b. DVM (ac) at  $E_1$  (term 6, U1) and across CRI.
- c. Audio signal generator in series with 5 k $\Omega$  resistor across CRI.

**TRIM PROCEDURE:** Set level of 1 kHz signal at Node CRI, R1, R2 to 0.1 V  $\pm 0.002$  V rms  
If  $E_1 > 0.852$  V rms, trim R2  
If  $E_1 < 0.848$  V rms, trim R6

### 2. THERMOMETER REFERENCE

**OBJECT:** Adjust R3 or R5 divider resistors such that  $E_1$  (term 6, U1) equals 4.120 V  $\pm 0.005$  V d.c. at 26°C. To correct for temperature difference between actual microcircuit temperature and 26°C use the formula  $E_1 = 4.120 + 0.018 (T_A - 26^\circ\text{C})$  where  $T_A$  is measured temperature of the microcircuit and 0.018 is the thermometer sensitivity in V/°C.

**CONDITIONS:**

- a. Regulated 9 V  $\pm 0.001$  V across 9 V interconnect and ground.
- b. DVM (dc) at  $E_1$  (term 6, U1)

**TRIM PROCEDURE:** If DVM  $> (E_1 \text{ corrected } +0.005 \text{ V})$ , trim R3  
If DVM  $< (E_1 \text{ corrected } -0.005 \text{ V})$ , trim R5

### 3. COMPENSATION DFG CURVE ROTATION

**OBJECT:** Adjust R56, R57 divider resistors to set voltage across R57 equal to 4.120 V such that the standard (design center) correction curve may be linearly rotated at the 26°C reference temperature.

**CONDITIONS:**

- a. Regulated 9 V  $\pm 0.001$  V across 9 V interconnect and ground.
- b. Branches containing R47 and R48 are open.
- c. DVM across R57

**TRIM PROCEDURE:** If DVM  $> 4.122$  V, trim R56.  
If DVM  $< 4.118$  V, trim R57.

### 4. COMPENSATING CURVE SELECTION

**OBJECT:** Select a compensating curve (described by a set of R47 and R48 values) from a family of rotated curves, by matching the frequency difference between upper and lower turning points (UTP-LTP) obtained from a corrected

F/T curve of the assigned crystal unit.

CONDITION: a. F/T curve for crystal unit obtained in test set with crystal load capacitance at 20 pF.

b. Available family of F/T curves previously generated by rotation of the standard curve ( $R47 = R48 = 10 \text{ K}$ ) using various combinations of R47 and R48 with crystal oscillator maintained at constant room temperature.

PROCEDURE: Correct for circuit F/T contribution by adding 3 ppm to crystal F/T curve (UTP-LTP) difference. (A near linear repeatable clockwise rotation of the crystal F/T characteristic is produced by the positive TC of the crystal load capacitance). Select a curve (set of R47 and R48 values) which will provide a frequency change equal to the corrected crystal F/T curve (UTP-LTP) difference.

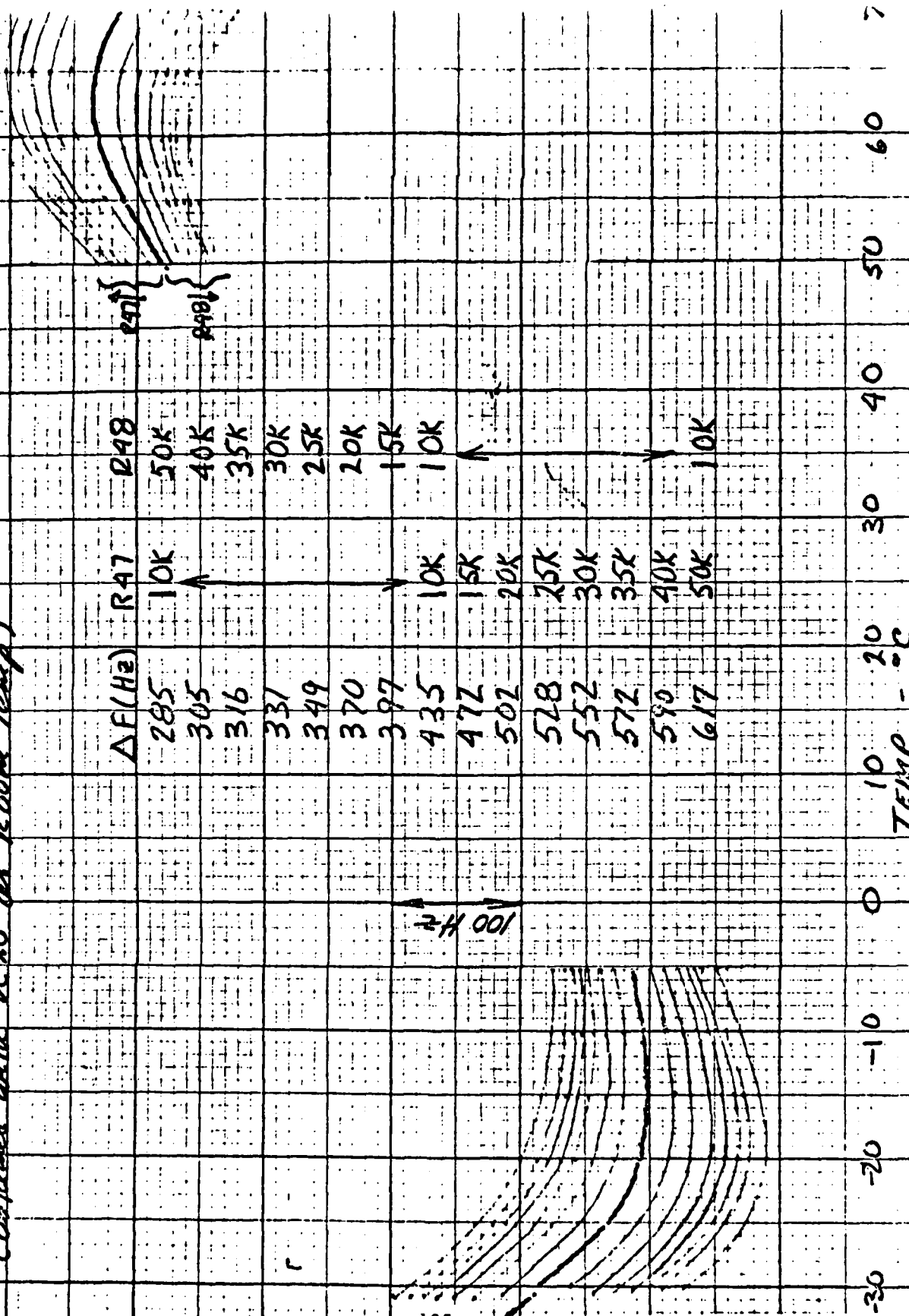
#### 5. COMPENSATING CURVE ADJUSTMENT.

OBJECT: Adjust R47 or R48 such as to provide the required rotated compensating F/T curve.

CONDITIONS: a. DVM (ohms) or resistance bridge across R47 or R48.  
b. Branches containing R47 and R48 are open.

TRIM PROCEDURE: Perform passive trim of R47 or R48 to within  $\pm 5\%$  of values determined in Step 4, "COMPENSATION CURVE SELECTION". As a final step, close branches containing R47 and R48.

# FAMILY OF COMPENSATING CURVES FOR HIGH CURRENT DIVIDER (Obtained with VC 10 at Room Temp)



CHANGES TO COMPENSATION NETWORK ADJUST AND TRIM PROCEDURE  
FOR LOW CURRENT DIVIDER CIRCUIT

1. THERMOMETER GAIN. Change gain from  $8.5 \pm 5\%$  to  $10 \pm 5\%$ . Change trim procedure to read:

If  $E_1 > 1.002$  V rms, trim R2.

If  $E_1 < 0.998$  V rms, trim R6

2. THERMOMETER REFERENCE. Change reference voltage  $E_1$  from  $4.120$  V  $\pm 0.005$  V at  $26^\circ\text{C}$  to  $4.355$  V  $\pm 0.005$  V at  $26.2^\circ\text{C}$ . Change formula for corrected  $E_1$  from  $4.120$  V +  $0.018$  (TA- $26^\circ\text{C}$ ) to  $E_1 = 4.355$  V +  $0.021$  (TA- $26.2^\circ\text{C}$ )

3. COMPENSATION DFG CURVE ROTATION. Change R57 voltage set from  $4.120$  V to  $4.355$  V, change trim procedure to read.

If DVM  $> 4.357$  V, trim R56

If DVM  $< 4.353$  V, trim R57

CHANGES TO VCXO NETWORK ADJUSTMENT AND TRIM PROCEDURE  
FOR LOW CURRENT DIVIDER CIRCUIT

1. COMPENSATION GAIN: Change  $F_s$  from  $20.50$  MHz to  $19.88$  MHz.

DIVIDER (LOW CURRENT)

HZ	Pd	Pd	Pd
141	10K	10K	10K
152	10K	35K	
162	10K	30K	
189	10K	25K	
214	10K	20K	
246	10K	15K	
293	10K	10K	
342	15K	10K	
377	20K	10K	
408	25K	10K	
432	30K	10K	
452	35K	10K	
469	40K	10K	

TP5-TP30

10K  
15K  
20K  
25K  
30K  
35K  
40K

**APPENDIX D**  
**CONFIRMATORY SAMPLE TESTING**  
**TEST PLAN**



AD-A086 022

RAYTHEON CO QUINCY MASS INDUSTRIAL COMPONENTS OPERATION F/G 9/5  
MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MMATE) PROGRA--ETC(U)  
APR 80 R M ZILBERSTEIN DAAB07-76-C-8119

UNCLASSIFIED

DELET-TR-76-8119F

NL

3 of 3

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10-10-80

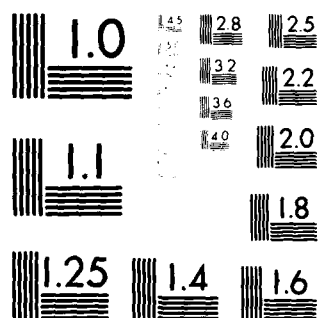
END

DATE

FILED

8-80

DTIC



MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-A

**PROCEDURE FOR  
CONFIRMATORY SAMPLE TESTING  
OF  
TEMPERATURE COMPENSATED, VOLTAGE CONTROLLED  
CRYSTAL OSCILLATOR  
SCS-483**

TCVCXO } - 1  
          } - 2  
          } - 3

**FOR**

**Communications Systems Procurement Branch  
P&P Directorate, U.S.A. ERADCOM  
Fort Monmouth, New Jersey 07703**

**AS REQUIRED BY**

**Item 0006 of Contract #DAAB07-76-C-8119  
as amended to Amendment #4**

**By:**

**Raytheon Company  
Industrial Components Operation  
465 Centre Street  
Quincy, MA 02169**

## TABLE OF CONTENTS

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2	Preconditioning and Screening Procedure	4
3	Confirmatory Test Procedures	7
 <u>Figures</u>		
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2	Temperature Test Set Up	14
3	Aging Set Up	15
Table II	Test Set Set-Up Chart	16

## **SECTION 1 - PURPOSE OF TEST PROGRAM**

To confirm the ability of the production facility to produce TCVCXO oscillators meeting the requirements of Amendment 4 of SCS-483 "ERADCOM Technical Requirements", a program is hereby set up to produce 50 oscillators in a production environment and to test them to determine the degree of compliance with the subject specification.

Modules will be produced, trimmed, and tested using materials, equipment, and techniques similar to those that will be used in high volume production.

Oscillators will be preconditioned and screened as described in Section 2 herein. This procedure is per MIL-STD-883, Method 5008, Class B, with the tests performed at the appropriate stage of the production process.

Finally, the oscillators will be tested according to Section 3 herein to determine the degree of compliance with the test requirements of the specification. Twenty-five (25) of the sample modules will be aged; the balance will be tested and shipped prior to aging, as required by contract.

## **SECTION 2 - PRECONDITIONING AND SCREENING PROCEDURE FOR TCVCXO OSCILLATORS PER SCS-483**

---

This process is intended to screen out defective devices by a series of tests performed at several steps of the production sequence. Together they include the required tests of MIL-STD-883, Method 5008, Class B, required by the contract and SCS-483.

Tests to be performed are as follows:

1.0 Pre-seal - to be performed on all TCFG and VCXO sub-assemblies.

1.1 Sub-assembly electrical test.

1.2 Bond Strength - Method 2011 - 100% for Confirmatory Samples.

1.3 Pre-cap visual inspection - Internal Method 2017, Test Condition B.

2.0 After Sealing - before mating of sub-assemblies.

2.1 Functional Electrical Test.

2.2 Stabilization Bake - Method 1008 - 24 hrs. @ 150°.

2.3 Temperature Cycle - Method 1010, Cond. B - 10 cycles.

2.4 Constant Acceleration - Method 2001, Cond. B - Y<sub>1</sub> axis only - 10,000G.

2.5 Seal Test - Fine and Gross - Method 1014, Cond. A and C, Limit  $1 \times 10^{-8}$  ATM cc/sec.

2.6 Visual Inspection - External - for catastrophic failures.

3.0 Tests performed after wiring together (but not epoxy bonding) TCFG, VCXO, XTL, and potentiometer to form functional TCVCXO.

3.1 Interim Electrical Tests.

3.1.1 Center Frequency.

3.1.2 Frequency Deviation  $\pm$  FSK Level Inputs.

## **Section 2 (Continued)**

- 3.1.3 Deviation Linearity.**
- 3.1.4 Regulated DC Output Voltage and Regulation.**
- 3.2 Burn-In - Method 1015 - 168 hrs. min. @ 125°C (except TCVCXO-1 @ 105°C).**
- 3.3 Interim Electrical Tests @ 25°C, +70°C and -40°C.**
  - 3.3.1 Center Frequency.**
  - 3.3.2 Frequency Deviation  $\pm$  FSK Level Inputs and  $\pm$  Analog Level Inputs.**
  - 3.3.3 Deviation Linearity.**
  - 3.3.4 Regulated DC Output Voltage and Regulation.**
- 4.0 Tests performed after completion of module assembly and potting.**
  - 4.1 Temperature Cycle - Method 1010, Cond. A except Temperature -40°C and +75°C, 10 cycles.**
  - 4.2 Final Test and Inspection.**
    - 4.2.1 For the Confirmatory sample modules, this will be performed according to Section 3 of this document. Detail procedures for automated production testing of modules will be prepared when automated test equipment becomes available.**

### SECTION 3 - CONFIRMATORY TESTS

All fifty (50) modules in the Confirmatory Sample will be subjected to the adjustment and test procedures numbered 1 through 15 of Table I. The lot will then be divided into two twenty-five (25) piece sub-groups. One half of the modules will be aged according to Test 16. The balance will be shipped without aging. Four reject modules will be subjected to Test 17.

TABLE I

<u>Test No.</u>		<u>Requirement Paragraph</u>
1	Frequency Adjustment	3.17
2	Center Frequency	3.9
3	Modulation Input Impedance	3.19
4	Frequency Deviation	3.20
5	Deviation Linearity	3.21
6	Input Power	3.23
7	Output Voltage - RF	3.24.1
8	Output Voltage - DC	3.24.2
9	Frequency - Temperature Stability	3.10
10	Frequency - Voltage Stability	3.11
11	Frequency - Load Stability	3.12
12	Transient Frequency Stability - Initial Turn On	3.13
13	Shock Sensitivity	3.15
14	Vibration Sensitivity	3.16
15	Modulation Bandwidth FSK and Analog	3.18
16	Aging Rate-Frequency-Time Stability	3.14
17	Terminal Durability	4.4



## DETAIL TEST PROCEDURE

For Confirmatory tests, to expedite delivery of product, a manually operated and recorded test set as shown in Figure 1 will be constructed. This will allow performance of most electrical tests. Peripheral equipment and circuitry will be needed for Test 9, 12 and 16.

### TEST PROCEDURES

- |   |  |
|---|--|
| <u>Test 1</u><br>Frequency<br>Adjustment<br>Range | Set up per Table 2 for Test 1.<br><br>Adjustment of frequency - adjust potentiometer in TCVCXO. Must allow at least +5 ppm adjustment around $F_c$ . Adjust pot to obtain frequency of $< 21,937,609$ Hz min. and the $> 21,937,390$ Hz max.   |
| <u>Test 2</u><br>Center<br>Frequency              | Adjust pot for $F = 21,937,500$ Hz.  |
| <u>Test 3</u><br>Input<br>Impedance               | With Mod. switch in Pos. 4, DC Meter SW Pos. 4, record voltage. Place Mod. SW in Pos. 3 and adjust decade resistor box for voltage one half of initial voltage. Record indicated resistance of decade box as Z in. Resistance must be $200K \pm 5\%$ - i.e. $190K\Omega$ to $210K\Omega$ . |
| <u>Test 4</u><br>Frequency<br>Deviation           | Measure frequency @ $2.500$ V + $0.625$ V FSK signal and @ $2.500$ V + $0.750$ V Analog signal input to Modulation input. Frequency shift must be $F_c \pm 312.5 \pm 10\%$ Hz and $F_c \pm 375 \pm 8\%$ Hz respectively.   |
| <u>Test 5</u><br>Deviation<br>Linearity           | Plot Frequency vs Control Voltage from data derived in Test 4 and Test 2, Center Frequency. Frequency measured at these levels must be within $\pm 5\%$ of the best straight line function plotted from Test 4, Frequency data.  |
| <u>Test 6</u><br>Input Power                      | With conditions per Step 6A then 6B (Table 2), press current meter switch and record current draw. Current must not exceed 4 ma @ 12 V (48 mw power limit) or @ 16 V.  |
| <u>Test 7</u><br>RF Output<br>Voltage             | Using a calibrated and compensated 10X scope probe, measure the RF voltage at the Direct RF Output Terminal. Output must be 1.0 V P-P minimum.   |
| <u>Test 8</u><br>DC Output                        | Under Test Cond. 8A through 8D (Table 2), DC output must be $9.000$ V DC $\pm 0.020$ Vdc at all test temperatures.   |

### TEST PROCEDURES (Continued)

**Test 9**  
**Frequency -**  
**Temperature**  
**Stability**

Set up test equipment and test set per Figure 2. Using cal  $-40^{\circ}\text{C}$  and cal  $+75^{\circ}$  switch, calibrate X axis range and zero controls on X-Y recorder at  $-40^{\circ}$  and  $+75^{\circ}$  points.

Using Audio Signal Generator, inject frequencies of 500 Hz, 800 Hz, and 200 Hz and calibrate Y axis range and zero controls on recorder to center, +300 Hz and -300 Hz on graph paper. Disconnect signal generator and connect mixer output to frequency meter.

Reference Oscillator is adjusted for a 500 Hz offset from nominal  $F_c$ . With test module at room temperature, the frequency meter should now indicate 500 Hz, and the recorder should indicate center frequency.

With module power off, place oven test box and oscillator in temperature chamber. Set cam at start  $-40^{\circ}\text{C}$  position and turn on refrigeration switch. After chamber temperature has reached  $-40^{\circ}\text{C}$ , allow 1/2 hour for stabilization, then turn on module power and allow an additional 5 minutes for stabilization.

Start timer programmer and temperature control cam and record frequency-temperature plot at  $F_o$ , Mark and Space frequencies from  $-40$  to  $+75^{\circ}\text{C}$ . Rate of temperature change shall be  $1^{\circ}\text{C}/\text{min}$ . or less. When temperature reaches  $+75^{\circ}\text{C}$ , turn off equipment and remove oscillator from oven.

Chart record should show a maximum frequency deviation at  $F_c$  of  $\pm 5$  ppm or  $\pm 110$  Hz max. for TCVCXO-1 and 2, or  $F_c \pm 25$  ppm or  $\pm 550$  Hz for - 3 over the temperature range. Mark and Space frequencies should be  $F_c \pm 312.5 \pm 10\%$  Hz at given temperature.

**Test 10**  
**Frequency/**  
**Voltage**  
**Stability**

Measure and record frequency with power supply voltage = 10.00 Vdc and @ 16.00 Vdc. Frequency shift must be less than  $\pm 0.25$  ppm or  $\pm 5.5$  Hz.

**Test 11**  
**Frequency/**  
**Load Stability**

Measure and record frequency when load is varied  $\pm 20\%$  from 1 K $\Omega$  center value. Set up 11A is 1K $\Omega$  load, 11B 1200K $\Omega$ , 11C 800K $\Omega$  load. Frequency shift not to exceed  $\pm 0.25$  ppm or  $\pm 5.5$  Hz.

## TEST PROCEDURES (Continued)

### Test 12 Transient Stability at Turn On

With test set per Test 12, adjust storage CRO trigger to DC + and adjust for triggering when Vcc switch is closed. Adjust discriminator and CRO Y axis sensitivity so that a shift of 10 Hz in/module output can be resolved. Set CRO time base for 10 ms/cm. Turn off Vcc switch for 30 sec., then reclose it, recording discriminator output on CRO. Frequency shift between 5 ms and 100 ms must be less than 10 Hz. Alternatively, function generator setup for 0-12 V 100 ms pulse width may be injected at TP with Vcc switch open.

### Test 13 Shock Sensitivity

Read Center Frequency @ 25°C. Then subject module to three (3) shocks at the required level:

- 1 100G 6 ms
- 2 1500G 0.5 ms
- 3 1500G 0.5 ms

in each of 6 MPP.

Immediately after the shock test, repeat frequency measurement. Frequency shift not to exceed 0.5 ppm (+11 Hz) due to shock test.

### Test 14 Measure Sensitivity

Measure output frequency @ 25°C. Subject module to the vibration test of MIL-STD-202 Method 204 Test Cond. B. Test requires vibration at 15G or 0.060 inch double amplitude over the frequency range 10-2000 Hz. Vibration is applied for 4 hours in each of 3 mutually perpendicular directions for a total of 12 hours.

At the completion of the vibration test and after module temperature has stabilized @ 25°C, repeat frequency measurement. Frequency shift due to vibration shall be less than  $\pm 0.25$  ppm or  $\pm 5.5$  Hz.

### Test 15 Modulation Bandwith

With set up per Test 15 A, B, and D, determine that modulation frequency deviation is down less than 3 dB at 8 kHz for analog (sine) signals and 1200 pps FSK signals. Test is made by examining the output of deviation meter as the signal frequency is varied with signal level held constant. Requirement is satisfied if discriminator output is  $>0.707 \times$  output at reference frequency ( $F_{ref} = 1$  kHz for sine, 100 Hz for FSK) - i.e. output less than 3 dB down at test pulse or analog rates.

### Test 16 Aging Rate - Frequency? Time Stability

With circuit per Figure 3, connect modules to test sockets and place in test tubes in controlled temperature bath.

Set bath temperature to  $60 \pm 0.1^\circ\text{C}$ . Set module power supplies to 12.000 Vdc and modulation voltage to 2.500 Vdc. After a two-week stabilization period, record oscillator frequency at 24-hour intervals (5 days per week). Oscillator frequency aging rate shall not exceed 1.25 ppm/week for TCVCXO-1 or  $2 \times 10^{-8}$ /week for TCVCXO-2 or -3 during the last week of aging test. Following this test, repeat Tests 4, 5, and 9.

### TEST PROCEDURES (Continued)

Test 17  
Terminal  
Durability

This test is substituted for Terminal Strength and Solderability Tests of Group C inspection, which cannot be performed on this type of terminal.

This test is to be performed on four (4) reject modules which have been through the Thermal Stress tests of pre-conditioning and screening. Samples need not be potted.

Step 1

Insert and withdraw connector of module into mating modified Amphenol #225-70621-101 spring contact socket using 1/16 inch G-10 spreader device to permit entry. Repeat insertion and withdrawal twenty (20) times total.

Step 2

Visual inspection of connector contacts for damage - 10X magnification.

Step 3

- A. Apply liquid rosin flux by brush to contact surfaces.
- B. Tin each contact by heating with 1/8 inch wide chisel type soldering iron tip with 30-47 watt heater and rosin core 60/40 solder.
- C. Remove flux using trichloroethylene or isopropyl alcohol.
- D. Visual inspection - 10X magnification - for dewetted or unsoldered areas in excess of 10% of tinned area.



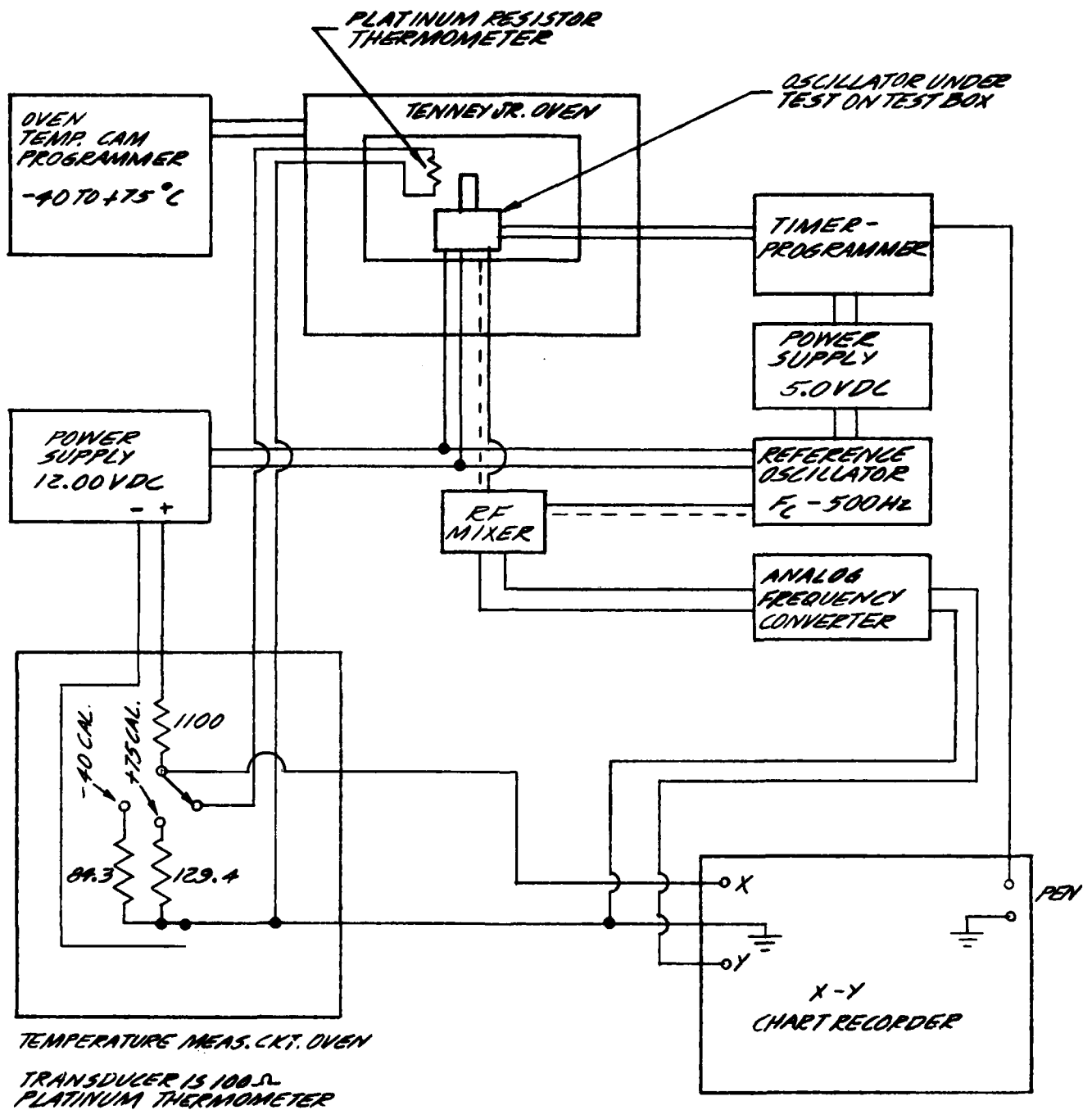
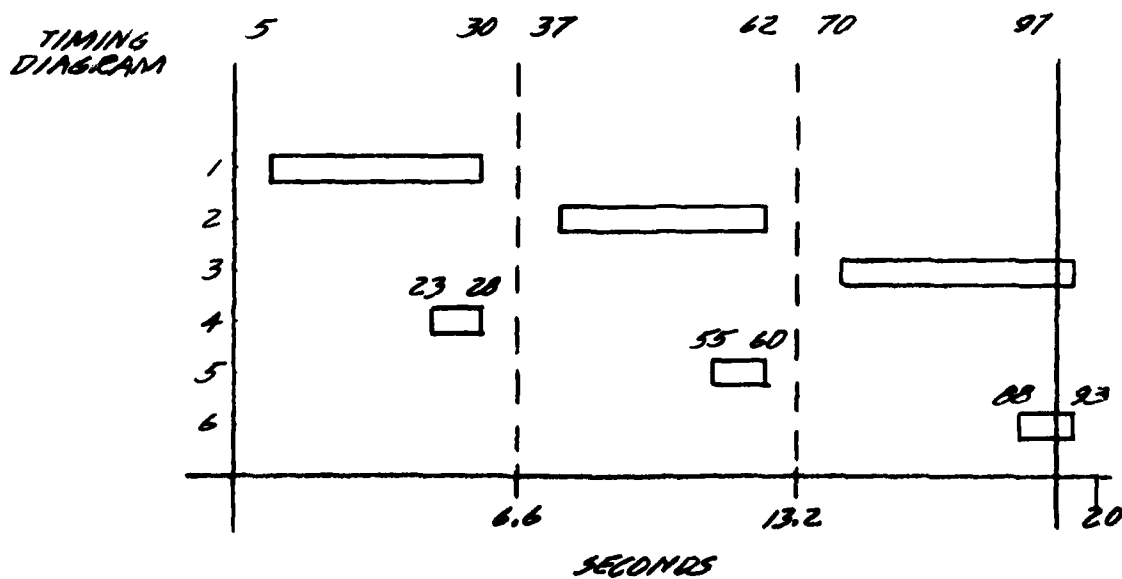
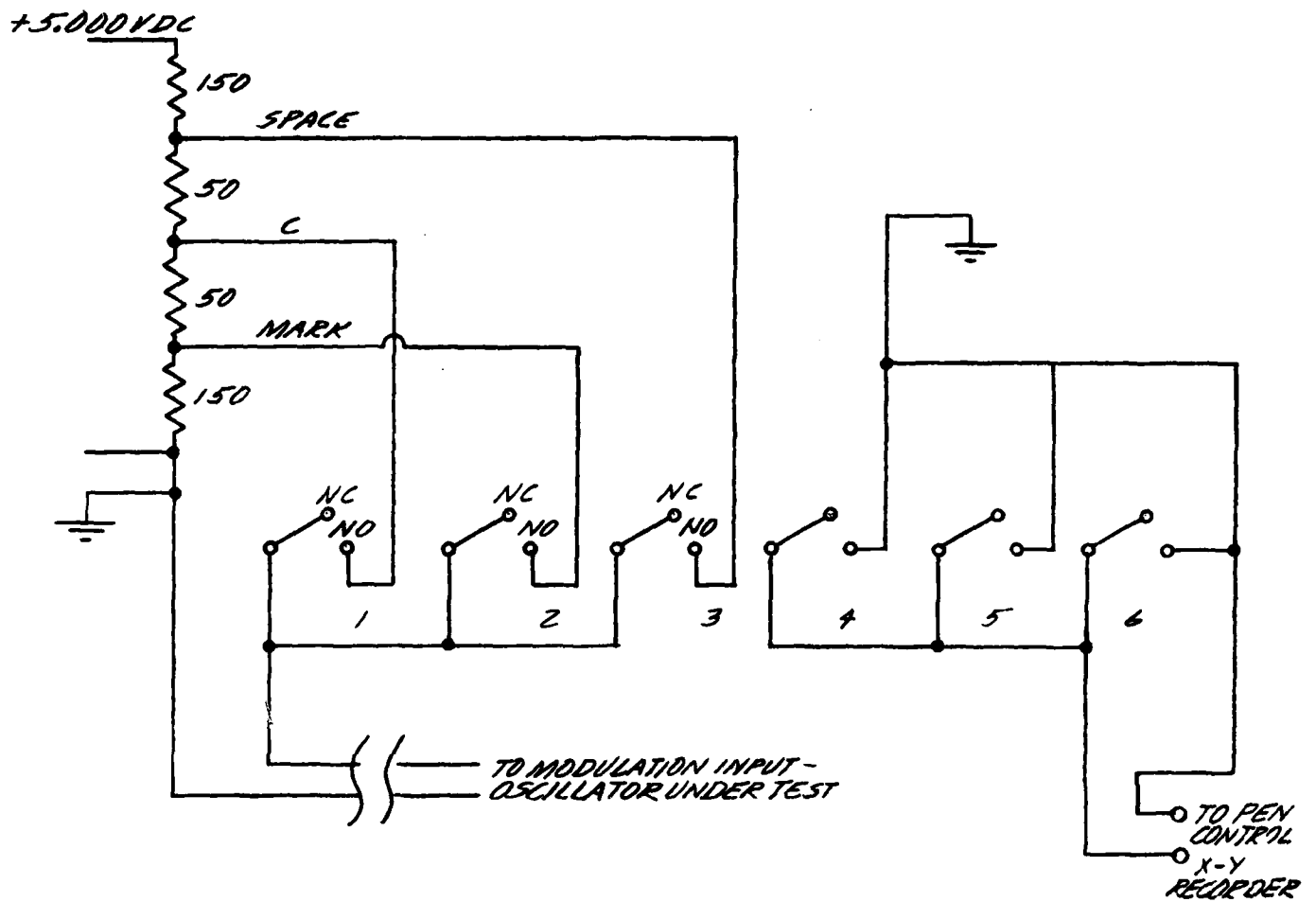
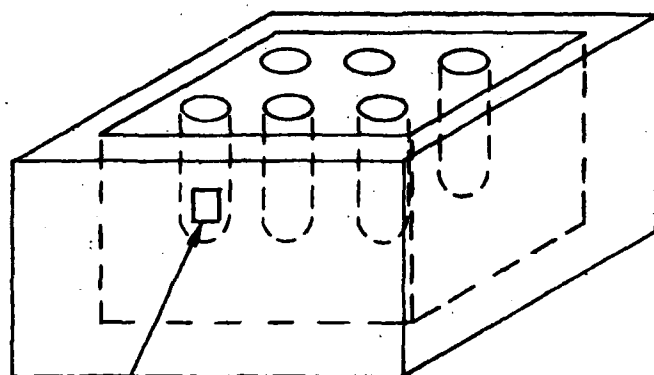


FIGURE 2  
FREQUENCY-TEMPERATURE TEST SET-UP

FIG. 2A  
20 SEC./CYCLE PROGRAM TIMER





MODULE UNDER TEST -  
ONE OF 64 IN BATH

BLUE M PRECISION  
WATER BATH  
MW 1216-C-1  
OR EQUIV.

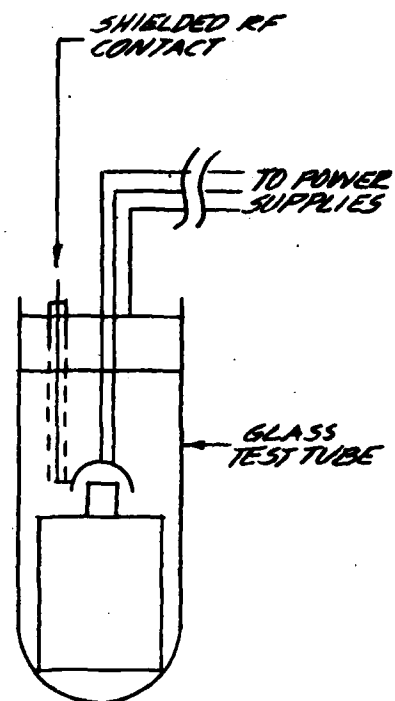
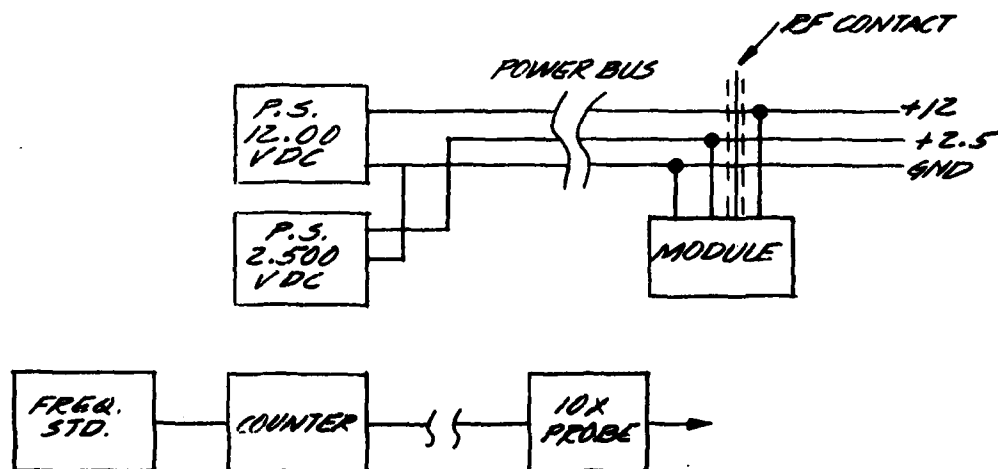



FIG. 3  
AGING SET-UP



TO MEASURE FREQUENCY TOUCH 10X PROBE  
TO RF CONTACT OF EACH MODULE IN  
SUCCESSION, RECORD FREQUENCY.



TABLE 2. TEST SETUP CHART TCVCXO

TEST#	DC METER SWITCH POSITION	POWER SUPPLY VOLTAGE	DC MODULATION VOLTAGE	FREQ. SHIFT LEVEL POS.	LOAD SWITCH POS.	INPUT SELECT SWITCH	REF. OSC	SCOPE A B	FUNCTION GENERATOR F form $V_1$ $V_2$
1	1 and 4	12.00	2.500	C	1	DC	off	off	
2	4	12.00	2.500	C	1	DC	off	off	
3	4	12.00	2.500	C	1	DC	off	off	
4A	4	12.00	2.500	C	1	DC	off	off	
B	4	12.00	3.125	S	1	DC	off	off	
C	4	12.00	1.875	M	1	DC	off	off	
D	4	12.00	3.250	A+	1	DC	off	off	
E	4	12.00	1.750	A-	1	DC	off	off	
6A	1	12.00	2.500	C	1	DC	off	off	
B	1	16.00	2.500	C	1	DC	off	off	
7	1	17.00	2.500	C	1	DC	off	off	
8A	2	12.00	2.500	C	1	DC	off	off	
B	3	12.00	2.500	C	1	DC	off	off	
C	3	10.00	2.500	C	1	DC	off	off	
D	2	16.00	2.500	C	1	DC	off	off	
9A	1	12.00	2.500	C	1	DC	off	off	
B	1	12.00	3.125	S	Use Test Setup Figure 2.		off	off	
C	1	12.00	1.875	M			off	off	
10A	1	10.00	2.500	C	1	DC	off	off	
B	1	16.00	2.500	C	1	DC	off	off	
11A	1	12.00	2.500	C	1	DE	off	off	
B	1	12.00	2.500	C	2	DC	off	off	
C	1	12.00	2.500	C	3	DC	off	off	
12	1	12.00	2.500	C	1	DC	on	Storage CRO and Discriminator Connect to RF Out. Trigger CRO @ TP.	
13	1	12.00	2.500	C	1	DC	on		
14	1	12.00	2.500	C	1	DC	on		
15A	Analog	12.00	n/A	n/A	1	Function Generator	on		Function 1-8 k Hz scan 3.1250 1.750 Generator 100-600 Hz scan 3.125 2.500 100-600 Hz scan 2.500 1.875 (5 ms → 0.833 ms pulse width) Connect Marconi Deviation Meter to RF Output.
B	Space FSK	12.00							
C	Mark FSK	12.00							
16	See Figure 3 Test Setup								

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